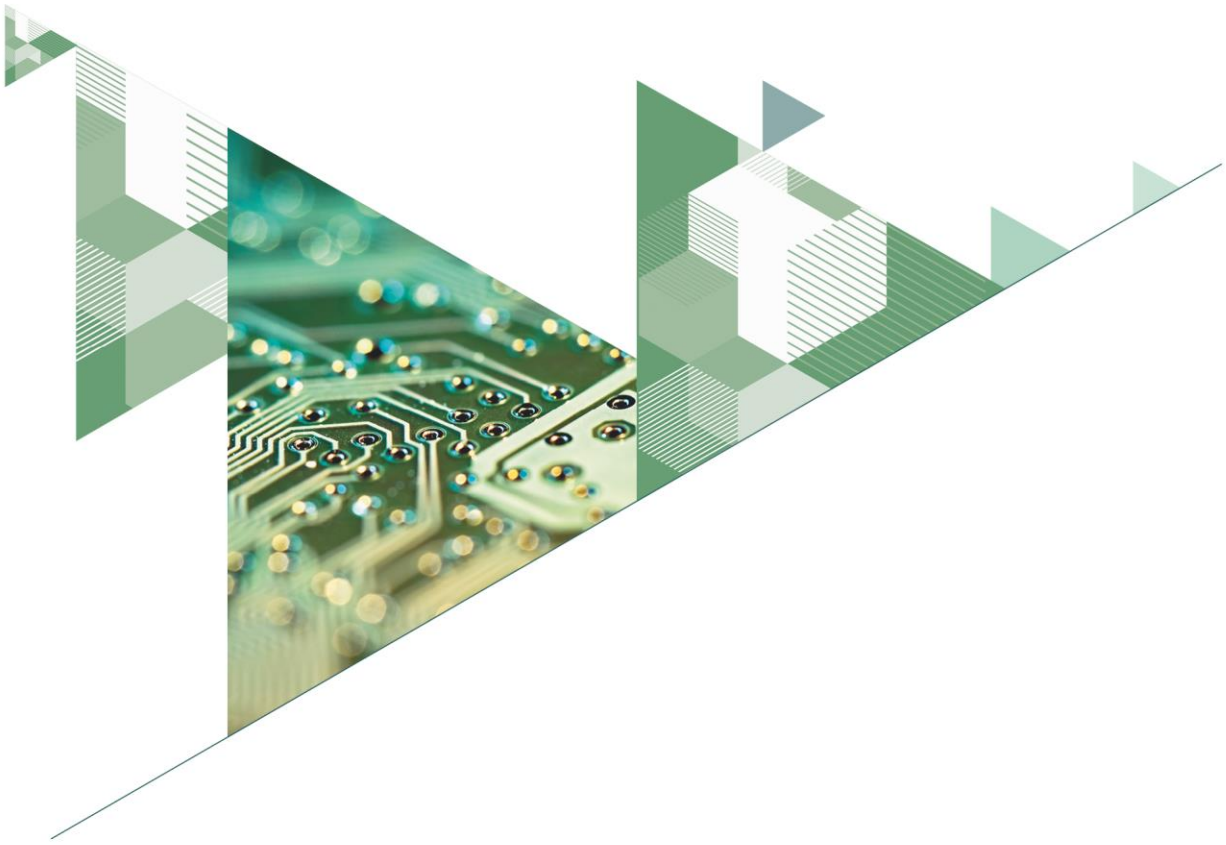


CGD65C025SP2 DATASHEET

P2 Series
650 V / 25 mΩ GaN HEMT with ICeGaN® Gate

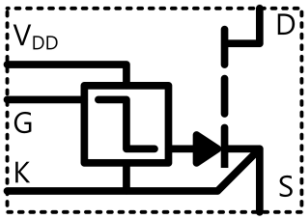
Document Number: CG-001808-DS
Issue 18 | 2025-11-21

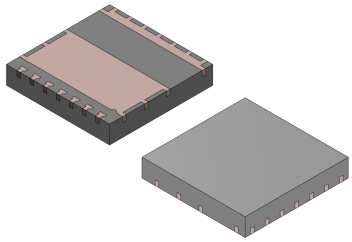
CGD™
CAMBRIDGE GaN DEVICES

P2 Series
650 V / 25 mΩ GaN HEMT with ICeGaN® Gate

Key features

- 650 V – 25 mΩ / 60 A eMode GaN power switch
- ICeGaN® gate technology for high gate threshold voltage, broad gate voltage window and excellent gate robustness
- Compatible with Si, SiC MOSFETs and IGBT drivers
- Gate drive voltage from 8 V to 20 V
- $R_{DS(on)}$ = 25 mΩ
- Integrated Miller Clamp for 0-V TurnOff
- Suitable for very high switching frequency
- Thermally enhanced bottom side cooled 10 × 10 mm SMD high power package
- Wettable flanks for automated optical inspection





Description

CGD65C025SP2 is a 650 V power transistor based on enhancement mode GaN for high power applications, delivering high current, impressive breakdown voltage, and high switching frequency. Central to its design is CGD's hallmark ICeGaN® gate technology which provides 3 V threshold voltage, genuine 0-V turn off, and a broad gate drive voltage range up to 20 V. This ensures compatibility with almost all available gate drivers and controller chips. Presented in a thermally optimised and compact 10 × 10 mm SMD package with wettable flanks, this power transistor is tailored for bottom side cooling and superior thermal resistance, making it ideal for multi-kW applications with demanding performance criteria.

Applications

- Industrial, data centre and telecom SMPS
- Industrial motor drives
- PV inverters
- Uninterruptible power supplies
- Energy storage systems

Topologies

- AC/DC and DC/DC converters based on single-ended, half-bridge, full-bridge and three-phase topologies with hard- and soft-switching
- Bridgeless Totem-pole PFC for the highest efficiency
- DC/DC resonant converters
- Buck and Boost converters
- DC/AC inverters

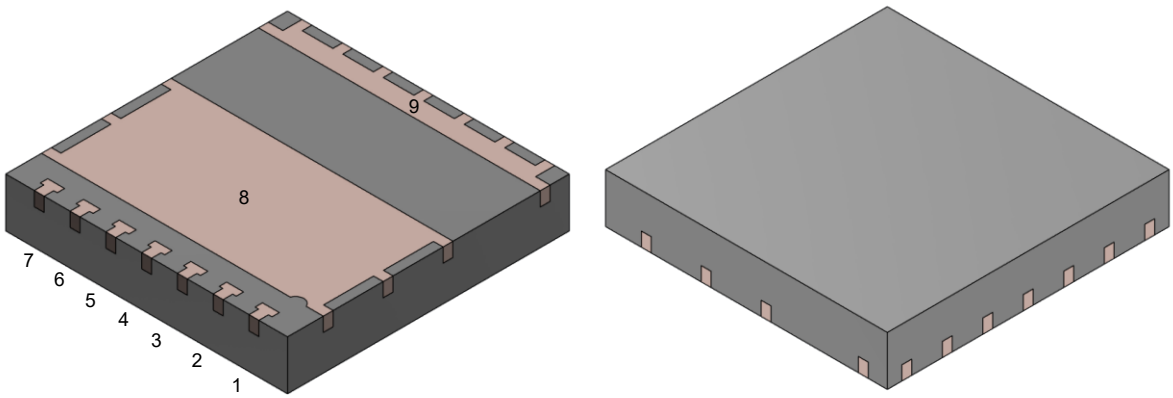


Figure 1. Package Image (Bottom View Left, Top View Right)

PIN	NAME	DETAILS
1, 2, 3, 4	Connect to Source	These package pins are not connected to the internal device but should always be connected to 'Source' via the PCB layout to minimise parasitics and noise and to maximise heat dissipation.
5	Kelvin Source	Kelvin source connection (internally tied to power HEMT source), reference potential for gate voltage.
6	Gate	Gate signal input. Recommended gate-drive voltage: V_{drive} (V_{GS} in on-state) = 11 V to 18 V or V_{DD} (if V_{DD} < 18 V).
7	VDD	ICeGaN® gate supply voltage (recommended 11-18 V), relative to Kelvin Source.
8	Source	Power HEMT source, thermal pad.
9	Drain	Power HEMT drain.

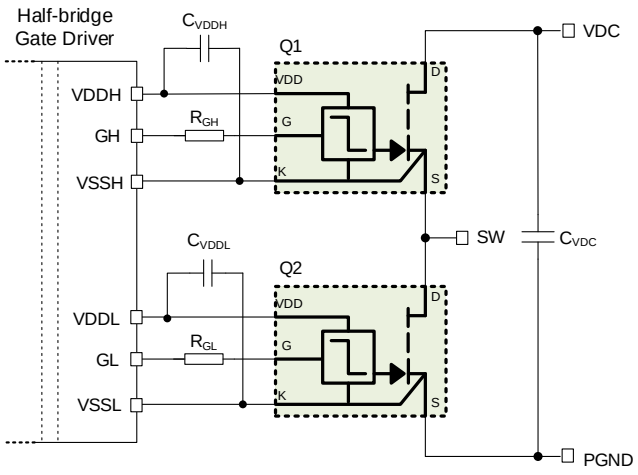


Figure 2. Example of an Application Circuit.

Absolute Maximum Ratings

T_{case} = 25 °C if not listed.

PARAMETER		VALUE	UNIT
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-Source Voltage	V_{DS}	650	V
Drain-Source Voltage - transient [1]	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-1 to +20 and $V_{GS} \leq V_{DD}$	V
Gate-to-Source Voltage – transient [2]	$V_{GS(transient)}$	-1.5 to +21.5 and $V_{GS} \leq V_{DD}$ + 1.5	V
ICeGaN® Gate Supply Voltage	V_{DD}	0 to +20	V
Continuous Drain Current (T_{case} = 25 °C)	I_D	60	A
Continuous Drain Current (T_{case} = 100 °C)	I_D	40	A
Pulsed Drain Current (10 µs, T_j = 25 °C)	I_{D_Pulse}	150	A
Pulsed Drain Current (10 µs, T_j = 150 °C)	I_{D_Pulse}	90	A

The on-state gate voltage must be above 8 V for ICeGaN circuit to work properly. The recommended range of operation for V_{drive} (V_{GS} in on-state) and V_{DD} is 11 V to 18 V for optimum performance, enabling simple integration with a large variety of control chips and gate drivers.

[1] Non-repetitive pulsed conditions, < 1 ms.
[2] Non-repetitive pulsed conditions.

Electrical Characteristics

Values at T_J = 25 °C, V_{DD} = 15 V if not listed. An integrated Miller Clamp eliminates the need for negative gate voltages.

STATIC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Drain-to-Source Blocking Voltage	BV_{DS}	V_{GS} = 0 V, I_{DSS} = 45 µA	650			V
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 15 V, I_D = 20 A		25	35	mΩ
Drain-to-Source On Resistance	$R_{DS(on)}$	T_J = 150 °C V_{GS} = 15 V, I_D = 20 A		65		mΩ
Source-to-Drain Voltage	$V_{SD(on)}$	V_{GS} = 0 V, I_D = 20 A		2.6		V
Gate-to-Source Threshold	$V_{GS(th)}$	V_{DS} = 0.1 V, I_D = 22 mA	2.2	2.9	4.2	V
Gate-to-Source Threshold	$V_{GS(th)}$	T_J = 150 °C V_{DS} = 0.1 V, I_D = 22 mA		2.6		V
Gate-to-Source Current	I_{GS}	V_{GS} = 15 V, V_{DS} = 0 V		3.6	5	mA
Gate-to-Source Current	I_{GS}	T_J = 150 °C V_{GS} = 15 V, V_{DS} = 0 V		4		mA
V_{DD} Current (V_{GS} in on-state)	I_{VDD}	V_{GS} = 15 V, V_{DS} = 0 V		1.4	2.5	mA
V_{DD} Current (V_{GS} in on-state)	I_{VDD}	T_J = 150 °C V_{GS} = 15 V, V_{DS} = 0 V		0.7		mA
V_{DD} Current (V_{GS} in off-state)	I_{VDD}	V_{GS} = 0 V, V_{DS} = 0 V		0.25	0.5	mA
V_{DD} Current (V_{GS} in off-state)	I_{VDD}	T_J = 150 °C V_{GS} = 0 V, V_{DS} = 0 V		0.25		mA
V_{DD} Start-up Current (V_{GS} in off-state)	I_{VDD_start}	V_{GS} = 0 V, V_{DS} = 0 V		250		µA
Drain-to-Source Leakage Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 650 V		1.5	45	µA
Drain-to-Source Leakage Current	I_{DSS}	T_J = 150 °C V_{GS} = 0 V, V_{DS} = 650 V		65		µA

DYNAMIC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Output Capacitance[3]	C_{OSS}	V_{DS} = 400 V, V_{GS} = 0 V f = 100 kHz		131		pF
Output Capacitance Stored Energy	E_{OSS}			16.3		µJ
Effective Output Capacitance, Energy Related[4]	$C_{O(ER)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		204		pF
Effective Output Capacitance, Time Related[5]	$C_{O(TR)}$			317		pF
Output Charge	Q_{OSS}	V_{DS} = 400 V, V_{GS} = 0 V		127		nC
Total Gate Charge[6]	Q_G	V_{DS} = 400 V, V_{GS} = 0...15 V, I_D = 20 A, I_G = 60 mA		11		nC
Reverse Recovery Charge	Q_{RR}			0		nC
Turn-on Switching Energy	E_{ON}	V_{DS}= 400 V, V_{DD}=V_{GS}=15 V, T_j=25 °C, I_D = 20 A $R_{g(on)}$ = 15 Ω, $R_{g(off)}$ =1 Ω L = 51 µH, L_p = 3 nH, see Figure 19 and Figure 20		72		µJ
Turn-off Switching Energy	E_{OFF}			17		µJ
Turn-on Delay Time	$t_{d(on)}$			7		ns
Turn-off Delay Time	$t_{d(off)}$			16		ns
Rise Time	t_r			9		ns
Fall Time	t_f			6		ns

ESD RATING

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ESD Withstand Rating	HBM	Human Body Model (per JEDEC JS-001-2017)	2000			V

Thermal Characteristics

Typical values unless otherwise specified.

PARAMETER		CONDITIONS	VALUE	UNIT
Thermal Resistance, Junction to Case	$R_{th(JC)}$		0.34	K/W
Reflow soldering temperature	T_{reflow}	MSL3	260	°C

[3] Evaluated using small-signal measurements.
[4] $C_{O(ER)}$ is the value of fixed capacitance that stores the same amount of energy as C_{OSS} when V_{DS} changes from 0 V to a given V_{DS}.
[5] $C_{O(TR)}$ is the value of fixed capacitance that takes the same amount of charging time as C_{OSS} when V_{DS} changes from 0 V to a given V_{DS}, assuming a constant-current charging process.
[6] Turn-on gate charge value is listed. Turn-off gate charge value would be lower, because ICeGaN® discharges the gate internally.

Figures

Figures at T_J = 25 °C, V_{DD} = 15 V if not specified.

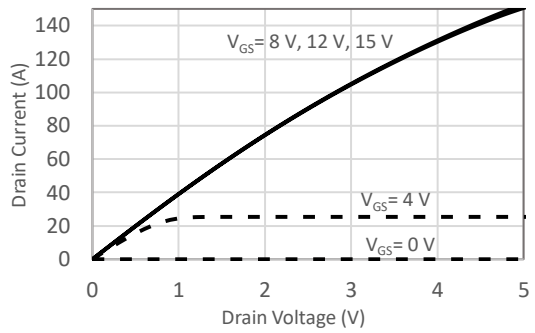


Figure 3. Forward output characteristics at T_J = 25 °C.

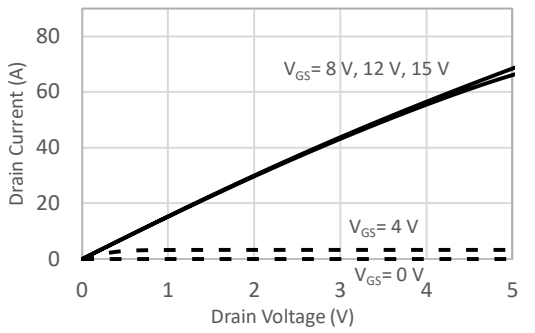


Figure 4. Forward output characteristics at T_J = 150 °C.

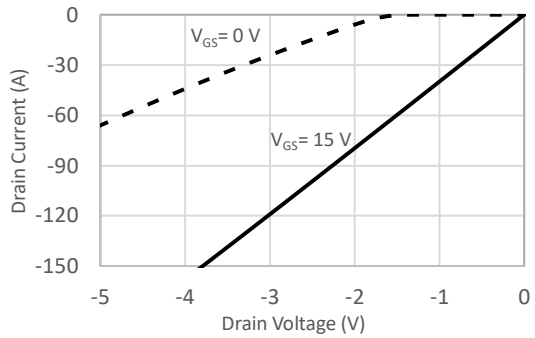


Figure 5. Reverse output characteristics at T_J = 25 °C.

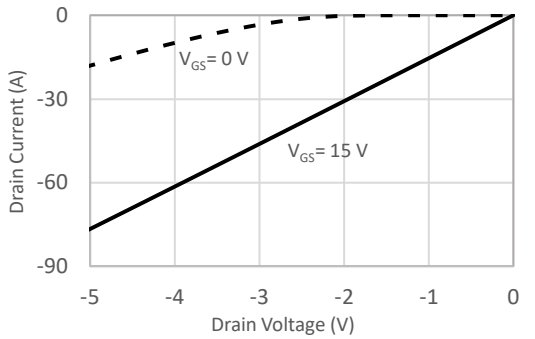


Figure 6. Reverse output characteristics at T_J = 150 °C.

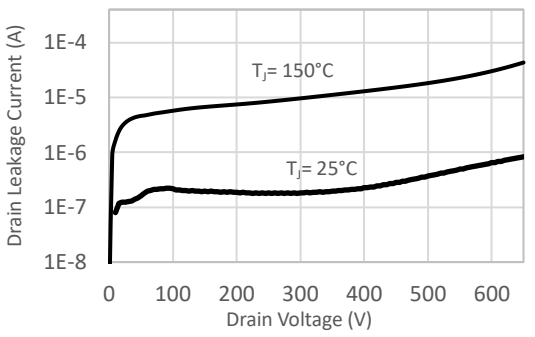


Figure 7. Drain leakage current characteristics at T_J = 25 °C and T_J = 150 °C.

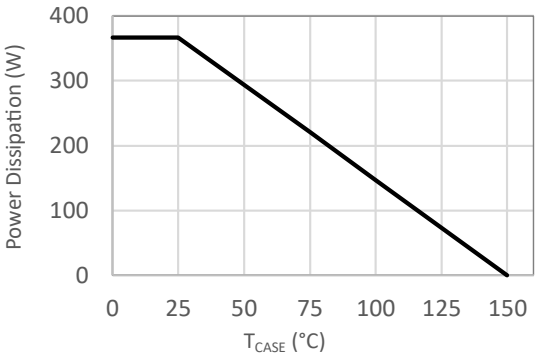


Figure 8. Power dissipation derating with case temperature.

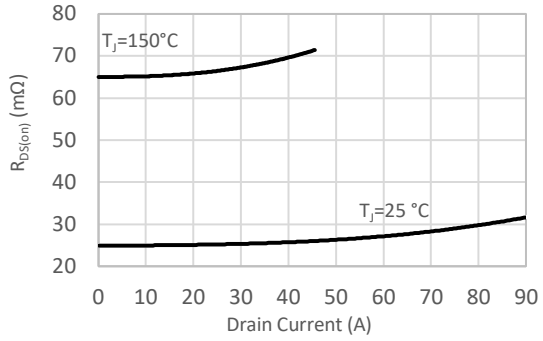


Figure 9. On-state resistance as a function of drain current at T_J = 25 °C and 150 °C at V_{GS} = 15 V.

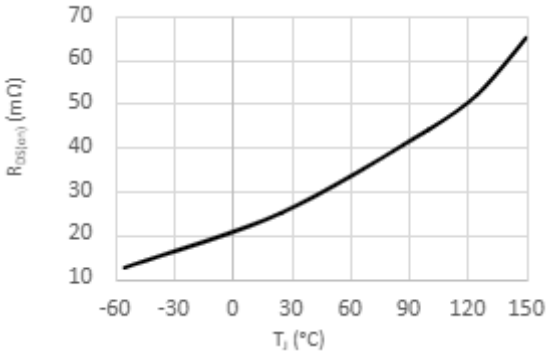


Figure 10. On-state resistance as a function of junction temperature at V_{GS} = 15 V.

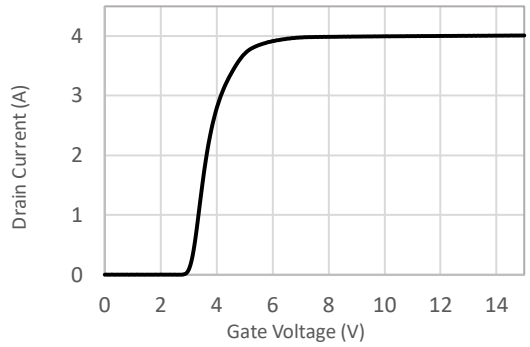


Figure 11. Transfer characteristics at V_{DS} = 0.1 V, T_J = 25 °C.

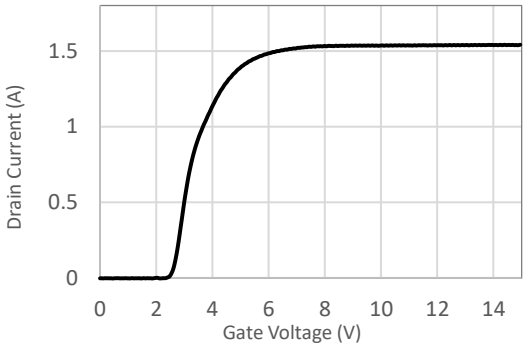


Figure 12. Transfer characteristics at V_{DS} = 0.1 V, T_J = 150 °C.

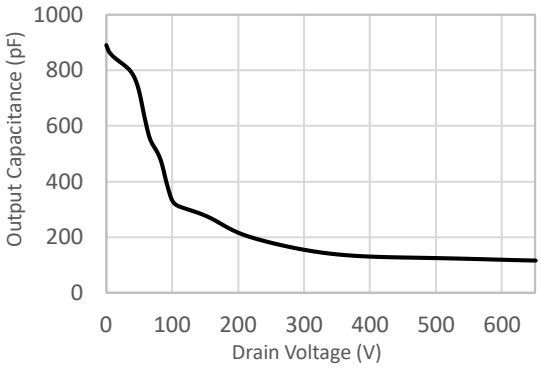


Figure 13. Typical output capacitance C_{OSS} vs. V_{DS} at 100 kHz, T_J = 25 °C.

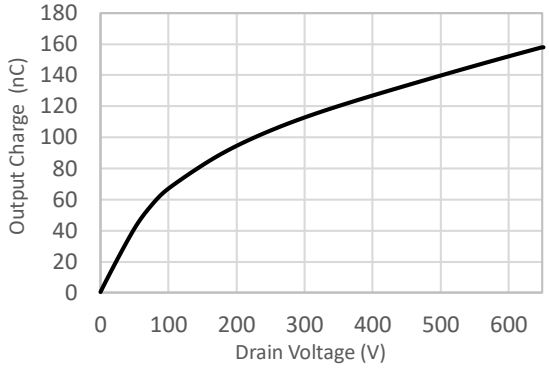


Figure 14. Typical output charge Q_{OSS} vs. V_{DS} at 100 kHz, T_J = 25 °C.

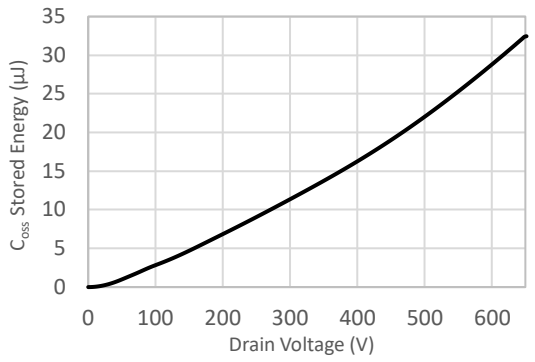


Figure 15. Typical C_{OSS} stored energy C_{OSS} vs. V_{DS} at 100 kHz, T_J = 25 °C.

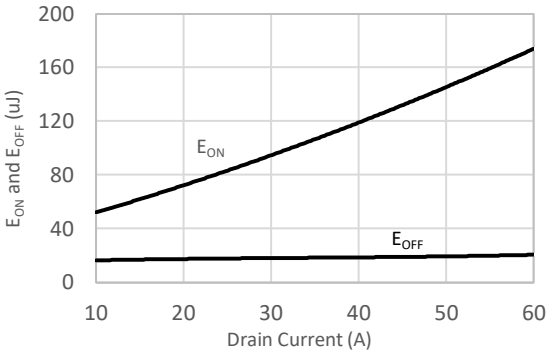


Figure 16. Switching energy vs I_{DS} at V_{DS} = 400 V, T_j = 25 °C.

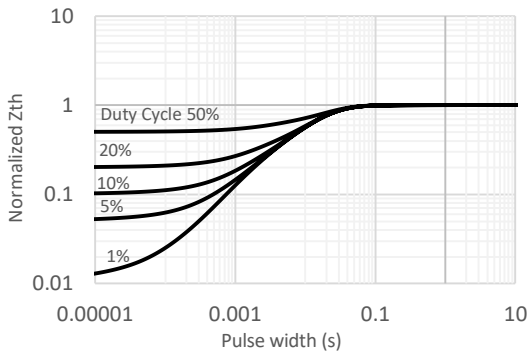


Figure 17. Normalized thermal transient impedance ($Z_{th,JC}$) as a function of pulse width.

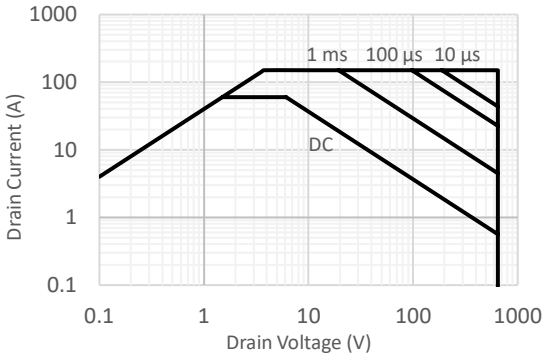


Figure 18. Safe Operating Area (SOA) based on thermal impedance $Z_{th,JC}$ at T_{case} = 25 °C.

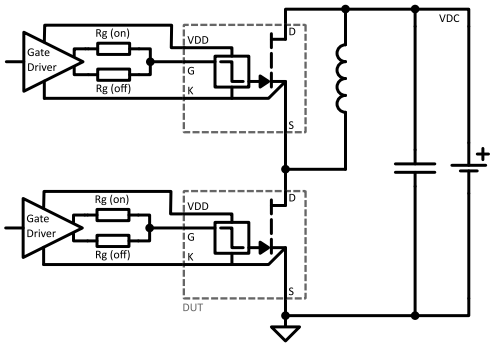


Figure 19. Inductive switching circuit. I_D = 20 A, $R_{g(on)}$ = 15 Ω, $R_{g(off)}$ = 1 Ω, V_{DD} = 15 V, V_{DC} = 400 V, L = 51 µH.

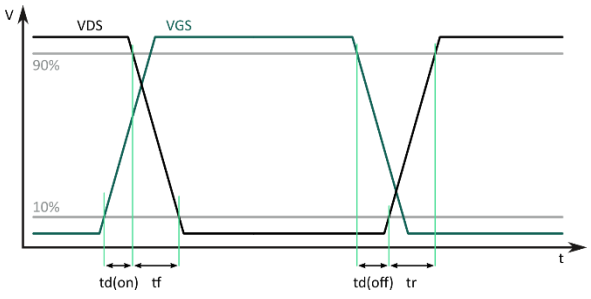


Figure 20. Switching waveform timing definitions.

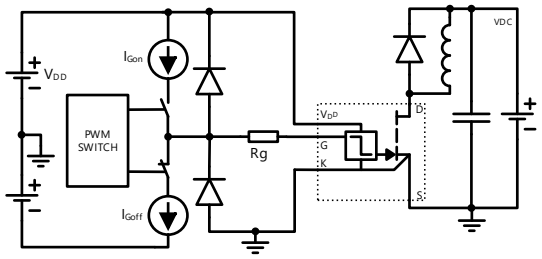


Figure 21. Q_G gate charge characterisation circuit. I_{Gon} = 60 mA, I_{Goff} = 60 mA, V_{DC} = 400 V, V_{DD}=15 V, L = 51 µH, Freewheeling Diode = C4D02120A.

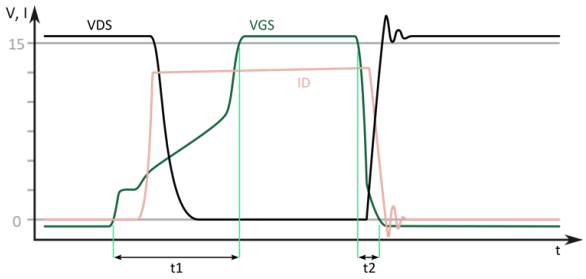
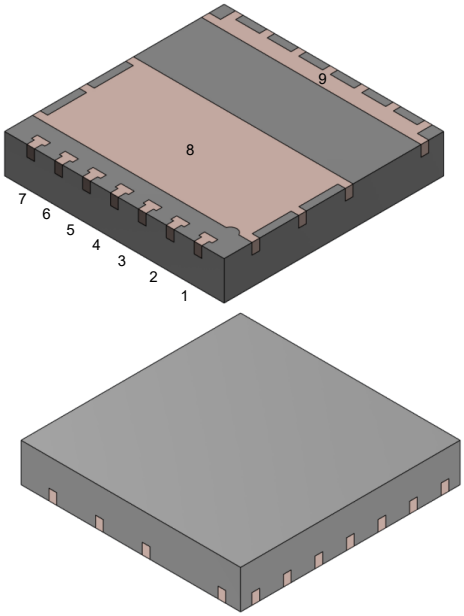


Figure 22. Q_G gate charge characterisation waveform at I_G = 60 mA and V_{DD} = 15 V. Time intervals t1 and t2 indicate the integration boundaries to calculate Q_G from I_G at turn-on and turn-off. Turn-off gate charge is lower than turn-on gate charge.

Packaging

Bottom-side cooled BHDFN-9-1 10 × 10 mm SMD.

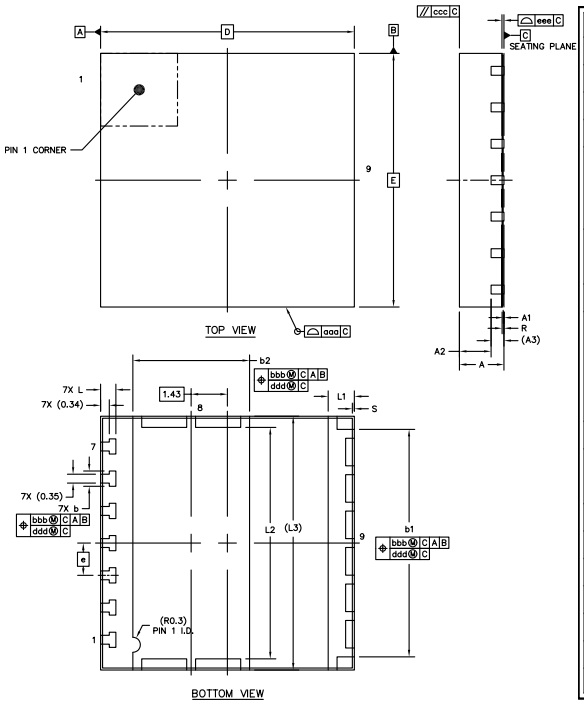
PIN NUMBER	NAME
1, 2, 3, 4	Connect to Source
5	Kelvin Source
6	Gate
7	VDD
8	Source
9	Drain



CGD65C025SP2 devices have the following marking on the package: 65Y1P2.

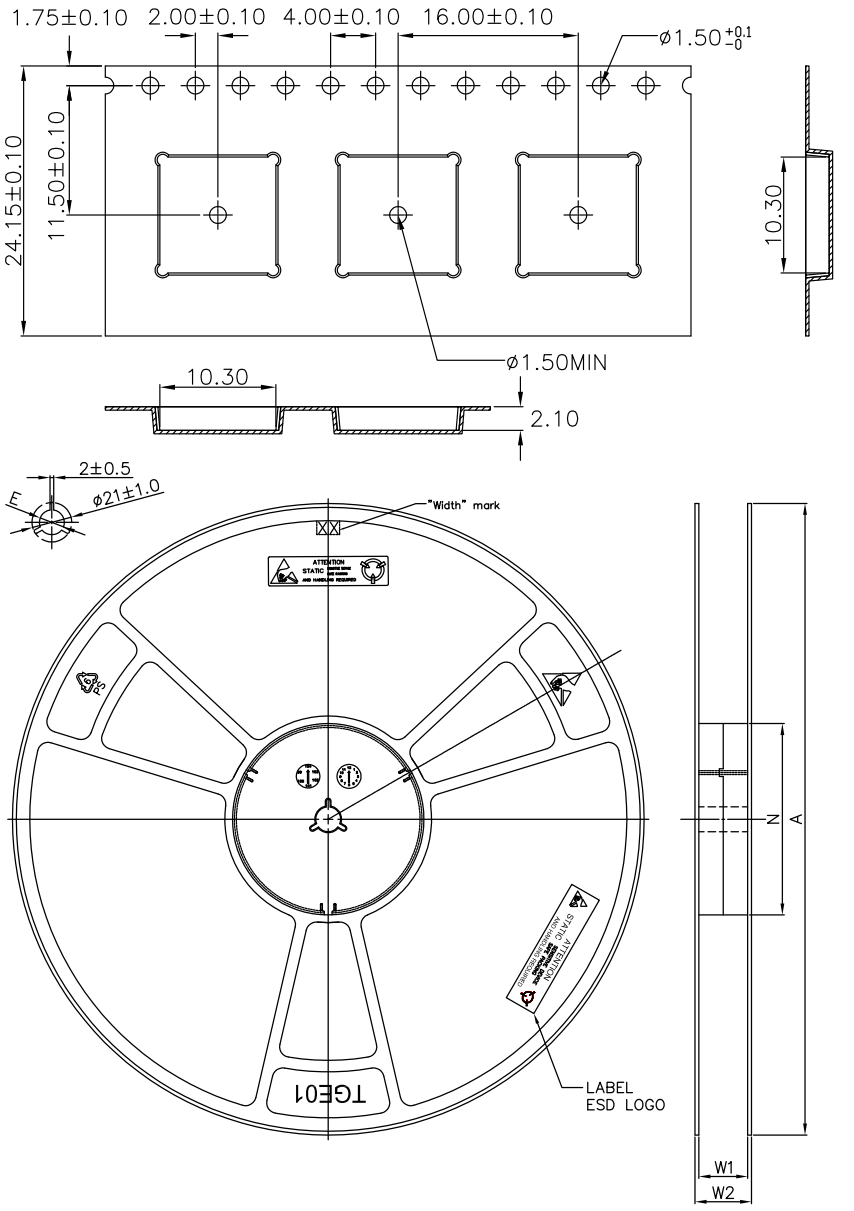
Like any unwanted electronic device, CGD components should be recycled or otherwise disposed of in accordance with local laws and regulations.

Package outline dimensions BHDFN-9-1 10 × 10 mm SMD.



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	1.7	1.75	1.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	1.25	---
L/F THICKNESS		A3	0.508		REF
LEAD WIDTH		b	0.5	0.6	0.7
		b1	8.87	8.97	9.07
		b2	4.5	4.6	4.7
BODY SIZE	X	D	10		BSC
	Y	E	10		BSC
LEAD PITCH		e	1.27		BSC
LEAD LENGTH		L	0.5	0.6	0.7
		L1	0.93	1.03	1.13
		L2	9.02	9.12	9.22
		L3	10		REF
PACKAGE EDGE TOLERANCE		aaa	0.15		
LEAD OFFSET		bbb	0.1		
		ddd	0.05		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
HALF-CUT DEPTH		R	0.075	---	---
HALF-CUT WIDTH		S	---	---	0.075

Tape and Reel Information



W	24.15 ±0.10
A0	10.30 ±0.10
B0	10.30 ±0.10
K0	2.10 ±0.10

TAPE WIDTH 24 mm	
	DIMENSIONS (mm)
A	330 ±2.0
N	100 ±2.0
E	13 ±0.2
W1	24.4 +2.0 −0
W2	29.4 ±1.0

Ordering Information

ORDERING CODE	PACKAGE TYPE	FORM	QUANTITY
CGD65C025SP2-T13	BHDFN-9-1 10 × 10 mm	Tape-and-Reel (13”)	1500

Version History

VERSION	DESCRIPTION	DATE	BY
1.0	Initial Release	15/07/2025	KM
17.0	• New version numbering scheme (prior version was 1.0) • Clarification to pin details provided for pins 1,2,3,4 in table on page 3	27/10/2025	JC
18.0	Minor Correction to Figure 10	21/11/2025	JC

Dare to innovate differently

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