ICeGaN® P2 HALF-BRIDGE EVALUATION BOARD

with Current Measurement Capability

User Guide

CGD-UG2601

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CAMBRIDGE GaN DEVICES

Safety Warning

The CGD half-bridge evaluation board (EVB) is for evaluation purposes only. It is not intended to be a finished product and does not include all protection features found in a commercial power supply. Only trained professionals experienced with high voltage equipment should operate the board and all appropriate safety precautions should be followed.

DANGER: Do not touch the board when high voltages are applied. There are exposed locations of high voltage on the board when connected to a power source. Brief contact may result in serious injury or death. Allow all components to fully discharge before handling the board. This evaluation board is designed for use by qualified, experienced engineers only. Appropriate safety measures must be put in place, and the board should never be left unattended.

WARNING: Some components may become hot during operation and remain so afterwards. Operating voltages, currents and temperatures should be monitored closely throughout operation to prevent damage to the board.

CAUTION: This product contains parts susceptible to ESD (electrostatic discharge). ESD prevention procedures must be used while handling the board.



Operating Limits and Recommendations

Heat dissipation

Heatsinking for the BHDFN ICeGaN® devices is provided through thermal vias in the source pad of each device to a heatsink mounted to the bottom side of the PCB. An electrically insulating thermal interface material (TIM) is placed between the exposed copper on the bottom layer of the PCB and a heatsink. An external fan may be required if continuous operational testing is desired.

Voltage Limits

This evaluation board was designed for a 400 VDC input bus, this being the most common bus voltage for 650 V rated devices. To test higher bus voltages, replace the 450 V electrolytic capacitor (C20) with an appropriately rated capacitor. Note that the ICeGaN® devices are rated at 650 V, while capacitors C16-C19 are rated to 630 V.

Target Audience

This guide, along with the board itself, is developed for experienced engineers and assumes a knowledge of necessary equipment and safety precautions to analyse the performance of the circuit board. It is designed to enable SMPS engineers, design engineers and technicians involved in the development of a power electronics system to rapidly assess the performance of CGD's ICeGaN®.

Technical Support

For support, please contact CGD at info@camgandevices.com.

Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	DSM	10/02/2026
1.1	Updated title for clarity	DSM	27/02/2026

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1 Board Overview

The ICeGaN® Evaluation Board (EVB) is designed to demonstrate the performance and ease of use of CGD's GaN technology. The EVB consists of two 650V GaN HEMTs configured as a half-bridge, and isolated gate drivers set to 15 V (the recommended drive voltage of ICeGaN). Optionally, this EVB can be supplied with an 11 mΩ current shunt to enable switching energy measurements (see section 2.4).

There are two products in the ICeGaN P2 series – CGD65C025SP2 (25mΩ) and CGD65C055SP2 (55mΩ). The user guide is applicable to both devices, since the inputs, configuration, and control of the EVB are identical.

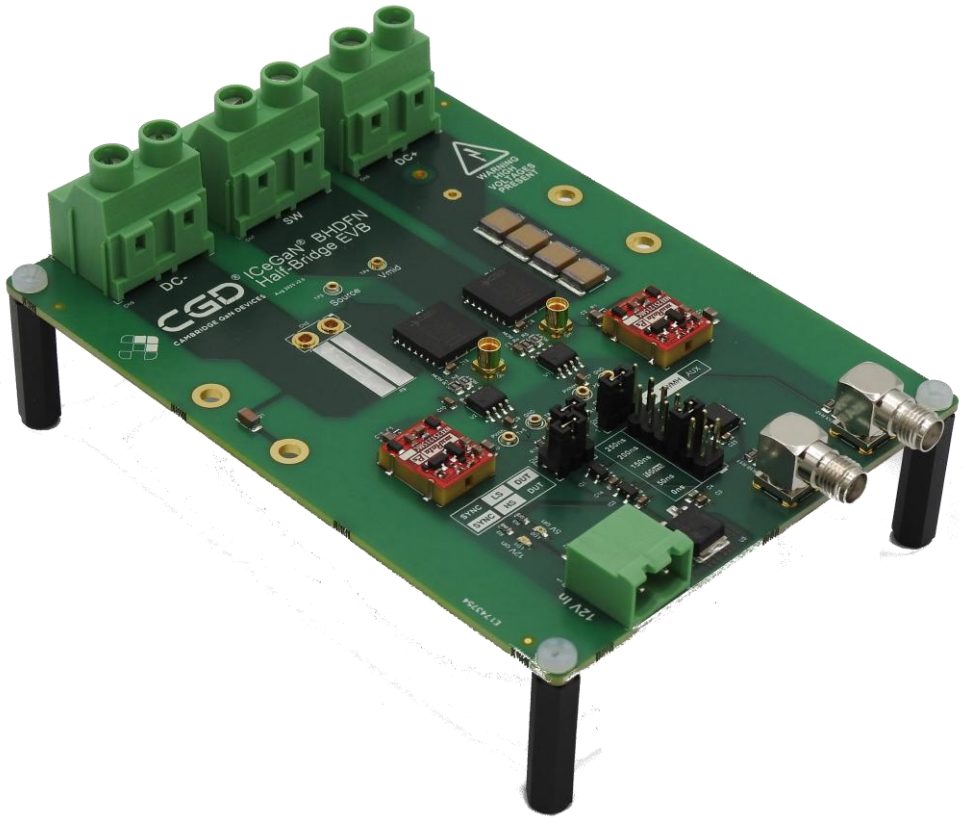


Figure 1 ICeGaN® Half Bridge Evaluation Board.

HB Board Part Number	CGD Devices	$R_{DS(on)}$ (mΩ)
CGD-ASYEVB02701-03	CGD65C025SP2	25
CGD-ASYEVB02702-02	CGD65C055SP2	55

Table 1 – Different board variations covered by this user guide.

1.1 Minimum Required Equipment

- High voltage DC supply
- 12 VDC supply (≥500 mA)
- PWM generation (controller, arbitrary waveform generator, etc)
- Suitable load inductor for testing
- Oscilloscope and high-voltage test probes

1.2 Power and Test Connections

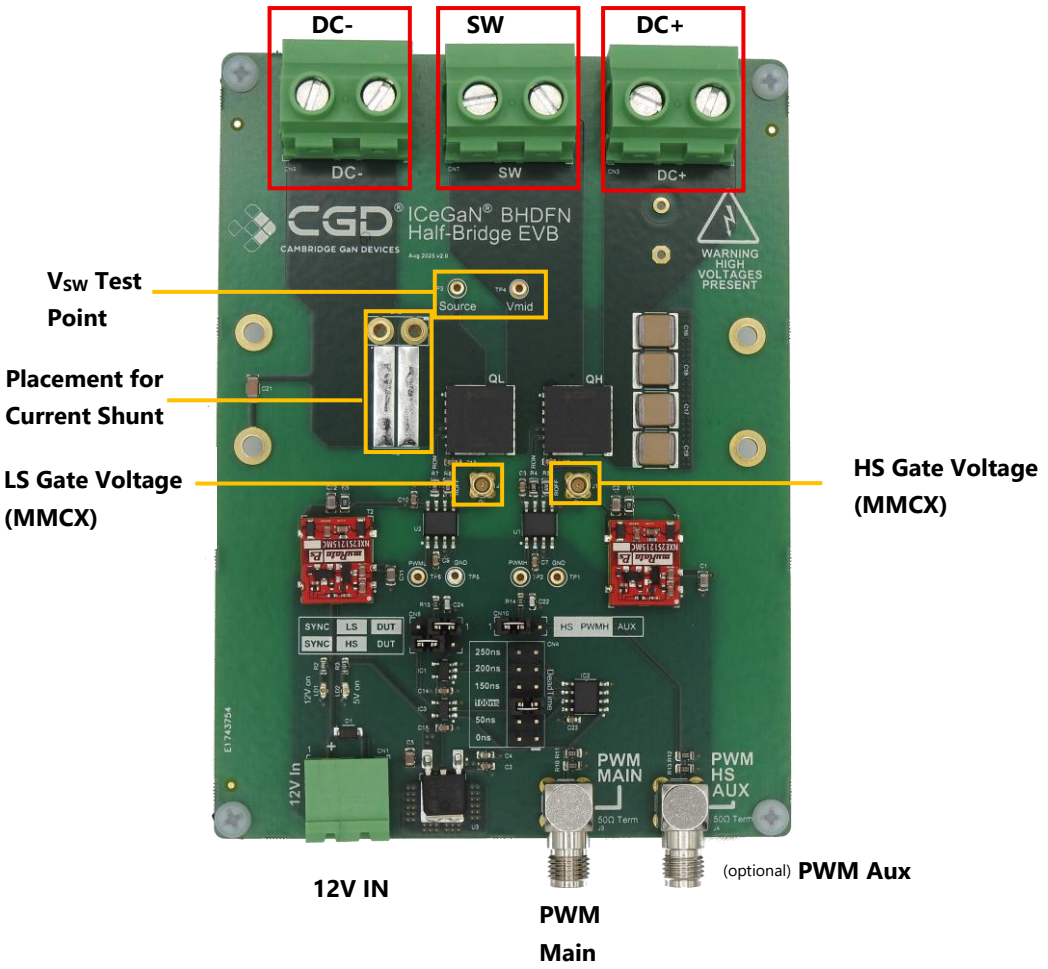


Figure 2 Key connectors and test points.

1.2.1 POWER AND SIGNAL INPUTS

Signal	Reference Designator	Connector	Comment
DC+	CN3	Terminal Block	HV input
SW	CN7	Terminal Block	Switch node of half bridge
DC-	CN9	Terminal Block	HV return
12V In	CN1	5.08mm header	12V supply input
PWM Main	J3	SMA	Main PWM input
PWM Aux	J4	SMA	Optional high side PWM input

Table 2 Half Bridge signal connections.

1.2.2 TEST POINT LOCATIONS

Signal	Reference Designator	Connector	Comment
V_{SW}	TP4 / TP3	Mill-Max	Low side (QL) V_{DS} (probe ground connected to source terminal of QL)
Source Current	CN2	Mill-Max	Opening for 5.08mm pitch current shunt
	R9	Surface mount	Pads for PMK UFCS current shunt
LS Gate	J2	MMCX	Low side ICeGaN gate
HS gate	J1	MMCX	High side ICeGaN gate
PWML	TP6 / TP5	Mill-Max	Low side PWM driver input
PWMH	TP2 / TP1	Mill-Max	High side PWM driver input

Table 3 Half Bridge test points.

Test Probe Grounding

Make sure that all the passive test probe grounds are referenced to the low side device's source or kelvin source. This is because with the current shunt placed, DC- will be at a different potential than the source terminal of QL. Also note that an isolated probe is necessary for measuring the high side gate voltage.

1.2.3 JUMPER SELECTION OPTIONS

Depending on the test requirements, the gate driver inputs can be configured in different ways. Refer to the tables below on how to configure the EVB.

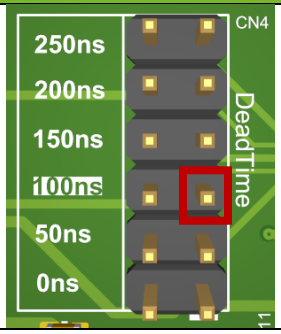
Dead Time for internal PWM			Pin Number	Name
	12	11	1	0 ns
	10	9	3	50 ns
	8	7	5 (red)	100 ns
	6	5	7	150 ns
	4	3	9	200 ns
	2	1	11	250 ns
			2,4,6,8,10,12	PWM w/ dead time

Table 4 CN4 connections.

For ease of testing, there is an internal dead time generation circuit on the EVB. When using PWM Main (J3) as the only PWM signal, connector CN4 sets the dead time generation between the high side and low side gate signals according to the table above. This dead time is set to 100 ns by default by shorting CN4.5 to CN4.6 via a jumper, as highlighted in the silkscreen and in Table 4.

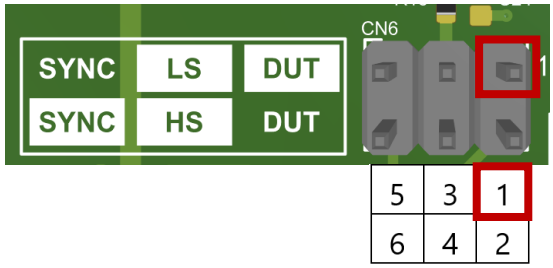
Internal PWM Selection	Pin Number	Name	Description
	1 (red), 2	DUT	PWM signal for the hard-switching device (DUT) in DPT.
	3	LS	To LS gate driver input pin.
	4	HS	High side PWM signal going to CN10 (see Table 6)
	5, 6	SYNC	Complementary DUT PWM signal for the soft-switching device in DPT (generated by dead time unit in Table 4).

Table 5 CN6 connections.

By default, the EVB is configured with the low side as the DUT (CN6.1 shorted to CN6.3 via a jumper) and the high side as the SYNC (CN6.4 shorted to CN6.6 via a jumper). This default configuration is highlighted in the silkscreen.

High Side control	Pin Number	Name	Description
	1 (red)	HS	Input from CN6 pin 4 (see Table 4)
	2	PWMH	High Side gate driver signal
	3	AUX	Input from J4 – PWM Aux

Table 6 CN10 connections.

The high side device can be driven from the internal dead time circuit (CN10.1 shorted to CN10.2 via a jumper) as highlighted in the silkscreen. Changing the CN10 jumper to the AUX input (CN10.2 to CN10.3) allows for arbitrary external PWM input to the high side device, bypassing the dead time unit.

2 Double Pulse Test (DPT) Results

The results below are for the CGD-ASYEVB02701-03 unit, which uses CGD65C025SP2 (650 V, 25 mΩ ICeGaN) devices. For testing with CGD65C055SP2 devices, the pulse widths for DPT will need to be adjusted to cater to the 55mΩ ICeGaN current rating.
The oscilloscope was set up as follows:

Signal	Trace Color	Vertical scaling	Probe Used
High Side Gate	Light blue	3 V/div	Tektronix ISoView 1GHz
Low Side Gate	Black	3 V/div	Tektronix TPP1000
V_{DS}	Red	70 V/div	PMK 711A
I_{DS}	Green	15 A/div	PMK UFCS 10mΩ shunt
Inductor Current	Dark Blue	15 A/div	Tektronix TCP0150

Table 7 Oscilloscope connections.

2.1 Test Conditions

Parameter	Value
V_{DC}	400 V
Inductor	51 µH (air core)
V_{DD}	15 V
$R_{G(on)}$	10 Ω
$R_{G(off)}$	2 Ω
Devices	CGD65C025SP2
Target Current	60 A

Table 8 Test parameters

Waveforms

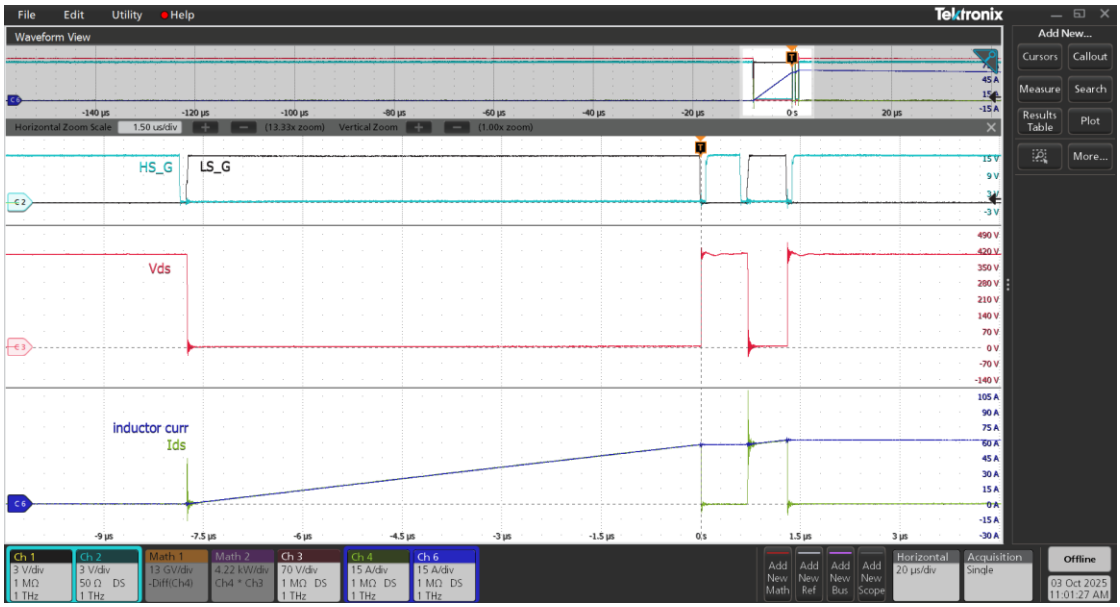


Figure 3 Experimental capture of 400V, 60A double pulse test with the low side as DUT.

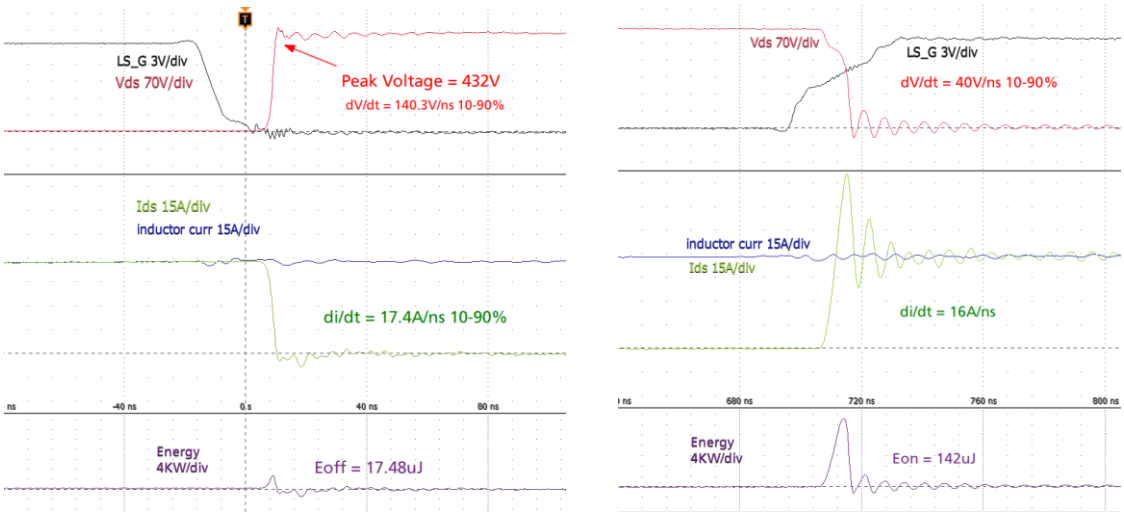


Figure 4 Turn off (left) and turn on (right) 400 V transitions in the DPT.

The waveforms from a 60 A double pulse test are shown above. Figure 3 shows the complete waveform and Figure 4 zooms in on the turn-on and turn-off events.

A high-bandwidth current shunt on the low side device enables measurements of the drain current during switching. The drain-source voltage was measured using a high-bandwidth, high-voltage passive probe. The VI overlap energy is then calculated using math functions on the oscilloscope. Repeating the DPT with different gate resistors, bus voltages, and inductor currents allows the designer to make decisions on balancing the driving of ICeGaN with the other factors in a system.

2.3 Probe Connections

V_{SW} = V_{DS}	Drain Current measured with UFCS
	
Low side (left) and High side (right) gate signals	
	

Table 9 Probe Connections.

2.4 Current Shunt Options

As mentioned in Section 2.2, the EVB was designed to allow for measuring the drain current of the low-side GaN HEMT. To achieve this, there are two options provided on the PCB for current shunts, shown below in Table 10.

The board will be shipped with R9 shorted, allowing for standard double pulse testing with no drain current measurement.

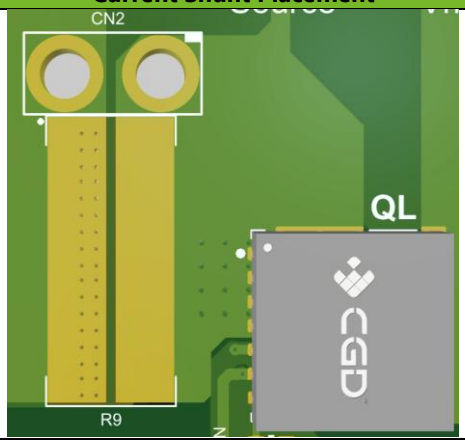
Current Shunt Placement	Ref Des.	Type
	CN2	Through-hole current shunt SDN-414
	R9	Surface mount current shunt PMK UFCS-R011

Table 10 Current shunt options.

Both options are high bandwidth (>1 GHz) solutions, which is needed for measuring the di/dt of ICeGaN and switching energies accurately. The major difference between the two options is the effect on the commutation loop inductance. Please contact CGD for additional information on the current shunt.

2.4.1 MEASUREMENTS

With fast switching HEMTs like ICeGaN, the power loop parasitics can cause ringing and overshoots on the current and voltage. The effect of this can be observed on the evaluation board by using the different current measurement options.

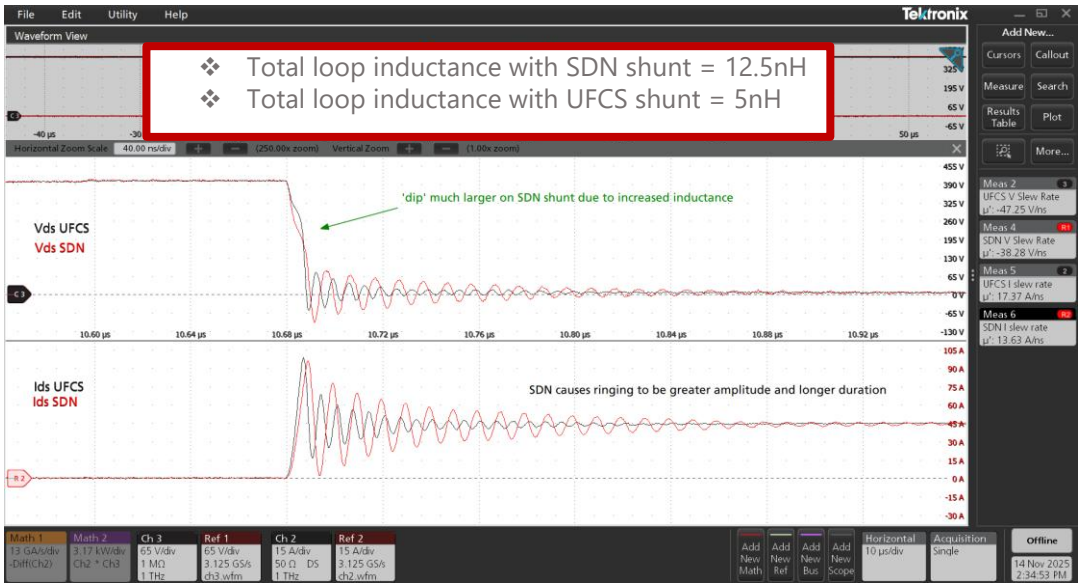


Figure 5 ICeGaN® hard-switching turn-on current shunt comparison.

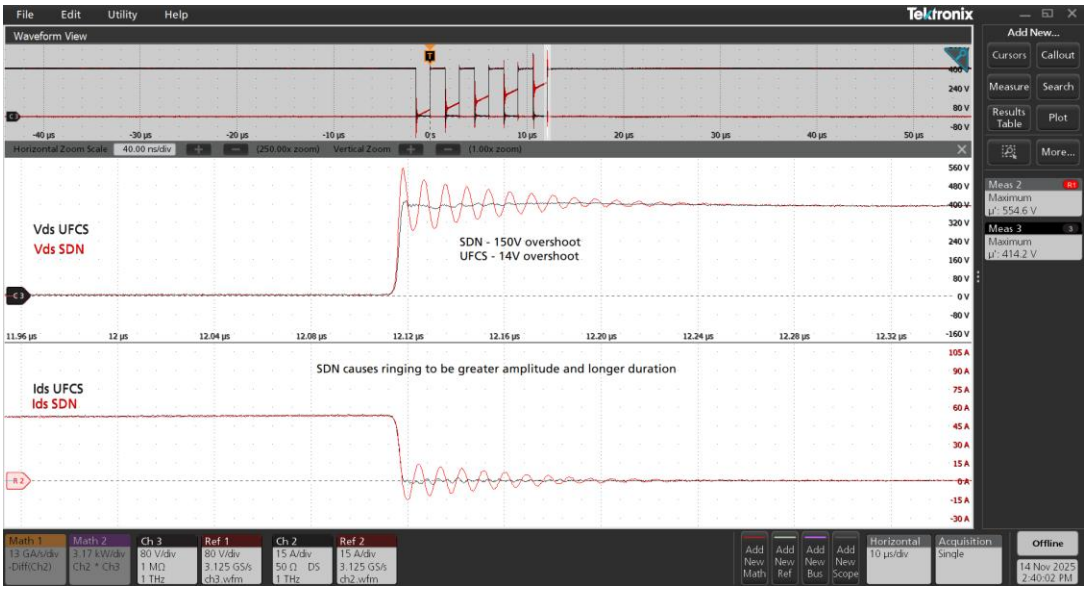


Figure 6 ICeGaN® hard-switching turn-off current shunt comparison.

The testing above in Figure 5 and Figure 6 was done with a 1 Ω gate resistor to amplify the effects of the power loop inductance. It is observed that the static measurements and transition edge timings are the same between the two options, but the amount of ringing and overshoot is dramatically affected by the greater than 2x increase in the loop inductance with the SDN option.

With the pads on the PCB, it is possible to have other options for the current measurement, for example: 1) placing a current sense resistor that is more applicable to a final design, or 2) soldering a wire to be used with a Rogowski coil. It is important to note that these options will affect the commutation loop differently.

3 Additional Resources

- ICeGaN® CGD65C025SP2 webpage
- ICeGaN® CGD65C055SP2 webpage
- ICeGaN® Evaluation Boards webpage

4 Schematic and PCB layout

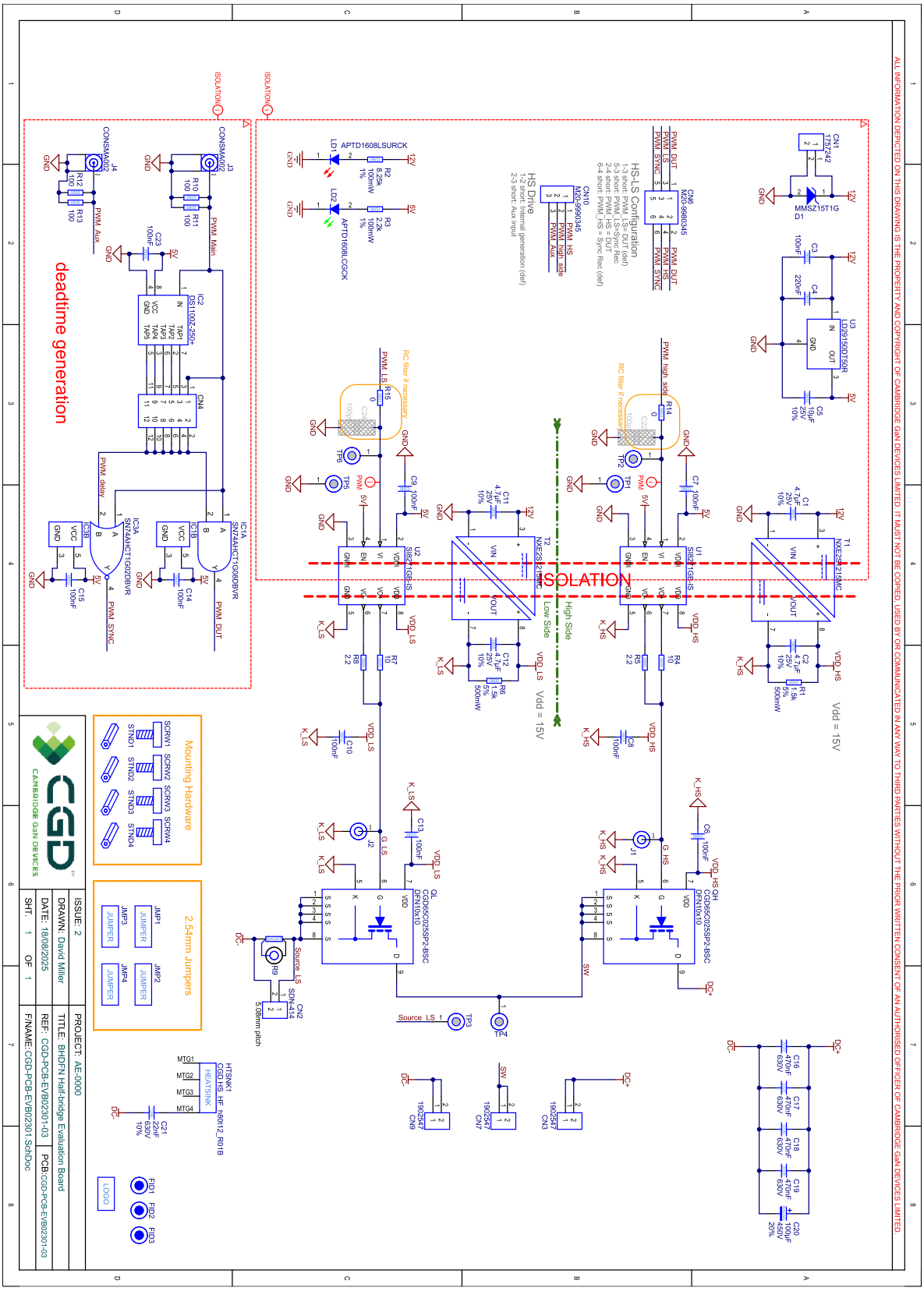


Figure 7 Half Bridge Evaluation Schematic

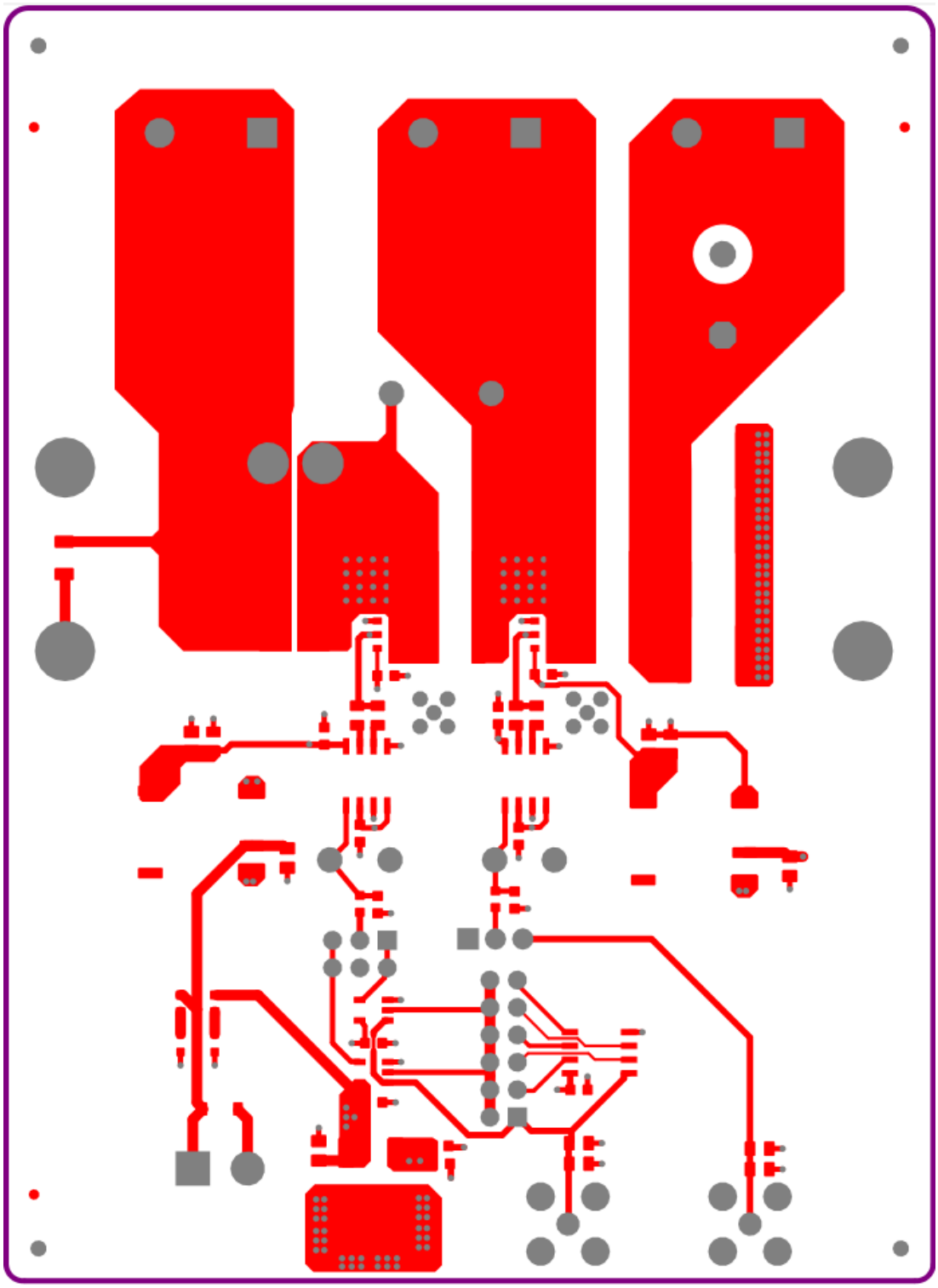


Figure 8 PCB Layer 1

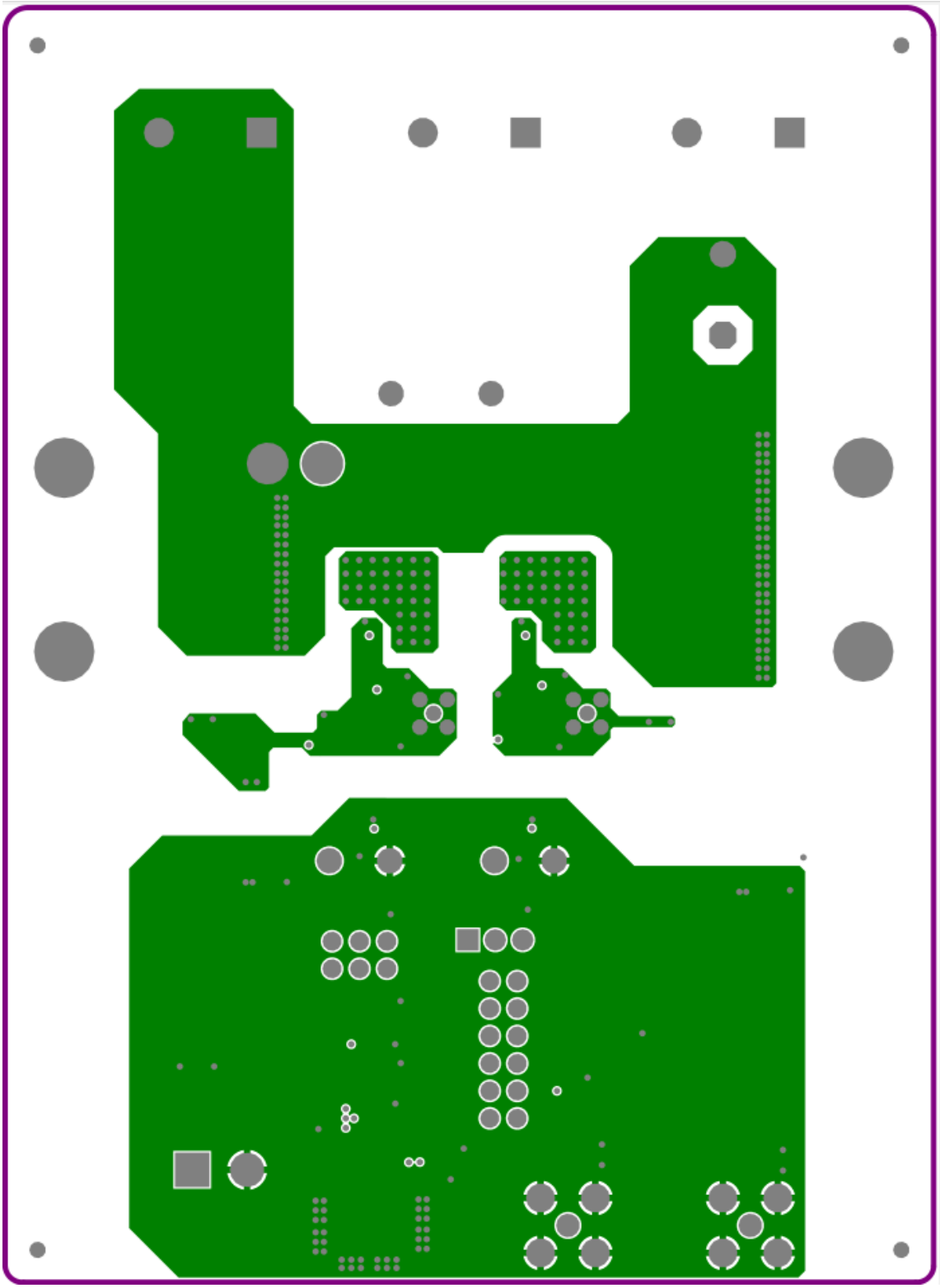


Figure 9 PCB Layer 2

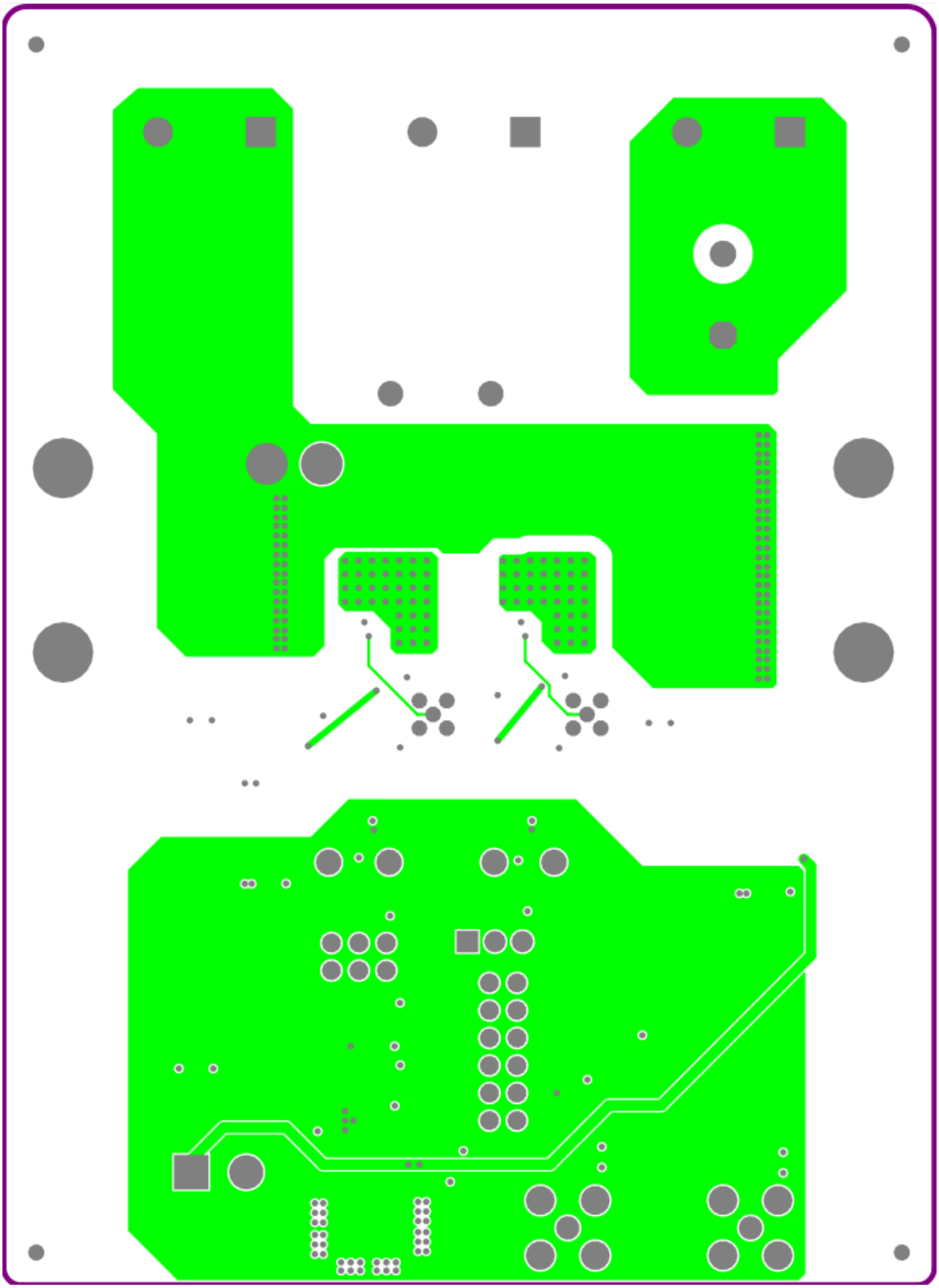


Figure 10 PCB Layer 3

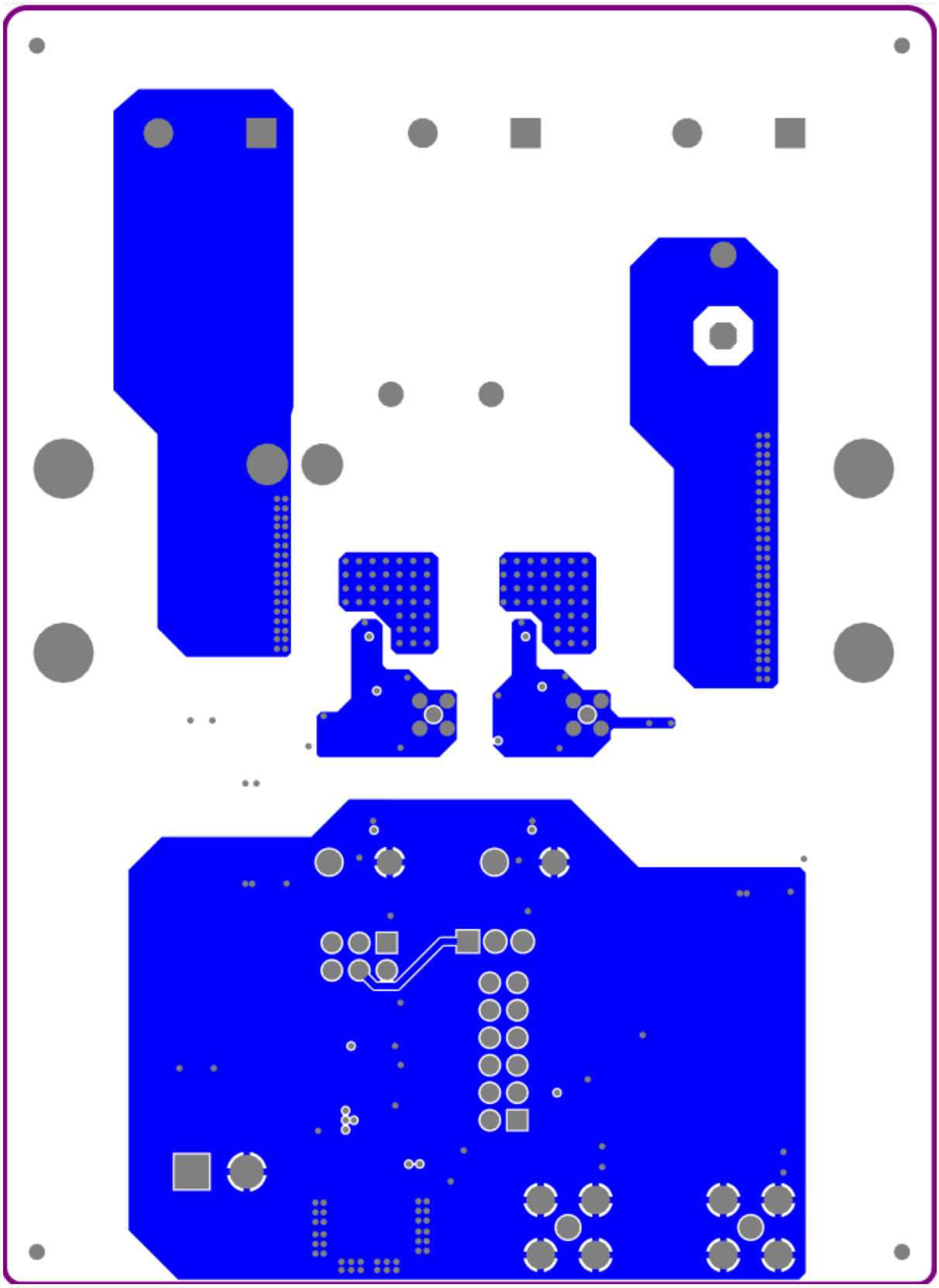


Figure 11 PCB Layer 4

5 Bill of Materials

Designator	Quantity	Description	Manufacturer	Manufacturer Part Number
C1, C2, C11, C12	4	4.7 µF ±10% 25V Ceramic Capacitor X7R 0805 (2012 Metric)	TDK	C2012X7R1E475K125AE
C3, C6, C7, C8, C9, C10, C13, C14, C15, C23	10	0.1 µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	Murata	GCM188R71H104KA57D
C4	1	0.22 µF ±10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	KEMET	C0603C224K3RACTU
C5	1	10 µF ±10% 25V Ceramic Capacitor X7S 0805 (2012 Metric)	Murata	GRT21BC71E106KE13L
C16, C17, C18, C19	4	0.47 µF ±10% 630V Ceramic Capacitor X7R 2220 (5750 Metric)	Murata	GRM55DR7LV474KW01K
C20	1	100 µF 450 V Aluminum Electrolytic Capacitors Radial, Can 3000 Hrs @ 105°C	Rubycon	450HXW100MEFR14.5X35
C21	1	0.022 µF ±10% 630V Ceramic Capacitor X7R 1206 (3216 Metric)	Yageo Group	CC1206KKX7RZBB223
CN1	1	2 Position Terminal Block Header, Male Pins, Shrouded (4 Side) 0.200" (5.08mm) 90°, Right Angle Through Hole	Phoenix Contact	1757242
CN2	1	Footprint for shunt receptacle, requires 2x Millmax 9372-0-15-15-23-27-10-0 receptacles	Mill-Max	9372-0-15-15-23-27-10-0
CN3, CN7, CN9	3	2 Position Wire to Board Terminal Block Horizontal with Board 0.375" (9.53mm) Through Hole	Phoenix Contact	1902547
CN4	1	Conn Unshrouded Header HDR 12 POS 2.54mm Solder ST Thru-Hole Bag	Harwin	M20-9980645
CN6	1	Conn Unshrouded Header HDR 6 POS 2.54mm Solder ST Top Entry Thru-Hole Bulk/Loose	Harwin	M20-9980345
CN10	1	Connector Header Through Hole 3 position 0.100" (2.54mm)	Harwin	M20-9990345
D1	1	Zener Diode 15 V 500 mW ±5% Surface Mount SOD-123	onsemi	MMSZ15T1G
HTSNK1	1	Heat Sink, CGD Custom, 80 mm, 25 mm, 12 mm	-	-
IC1	1	AND Gate IC 1 Channel SOT-23-5	Texas Instruments	SN74AHCT1G08DBVR
IC2	1	Delay Line IC Nonprogrammable 5 Tap 250ns 8-SOIC (0.154", 3.90mm Width)	Analog Devices	DS1100Z-250+
IC3	1	NOR Gate IC 1 Channel SOT-23-5	Texas Instruments	SN74AHCT1G02DBVR
J1, J2	2	RF Connectors / Coaxial Connectors MINI PUSH-ON CONN RECEPT STR	HIROSE ELECTRIC	MMCX-R-PC(40)

J3, J4	2	SMA Connector Receptacle, Female Socket 50 Ohms Through Hole, Right Angle Solder	TE Connectivity / Linx Technologies	CONSMA002
LD1	1	Red 630nm LED Indication - Discrete 1.75V 0603 (1608 Metric)	Kingbright	APTD1608LSURCK
LD2	1	Green 570nm LED Indication - Discrete 1.9V 0603 (1608 Metric)	Kingbright	APTD1608LCGCK
QH, QL	2	10x10mm – BHDFN ICeGaN®	CGD	CGD65C025SP2 **OR** CGD65C055SP2
R1, R6	2	1.5 kOhms ±5% 0.5W, 1/2W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	Panasonic	ERJ-P06J152V
R2	1	8.25 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	Yageo Group	RC0603FR-078K25L
R3	1	2.2 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	Yageo Group	RC0603FR-072K2L
R4, R7	2	10 Ohms ±1% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Moisture Resistant Thick Film	Yageo Group	RC0805FR-0710RL
R5, R8	2	2.2 Ohms ±1% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thick Film	Stackpole Electronics	RMCF0805FT2R20
R10, R11, R12, R13	4	100 Ohms ±1% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Moisture Resistant Thick Film	Yageo Group	RC0805FR-07100RL
R14, R15	2	0 Ohms Jumper 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	Stackpole Electronics	RMCF0603ZT0R00
T1, T2	2	Isolated Module DC DC Converter 1 Output 15V 133mA 10.8V - 13.2V Input	Murata Power Solutions	NXE2S1215MC-R7
TP1, TP2, TP3, TP4, TP5, TP6	6	Pin Receptacle Connector 0.025" ~ 0.037" (0.64mm ~ 0.94mm) No Tail Solder	Mill-Max	0305-2-15-15-47-27-10-0
U1, U2	2	4A Gate Driver Capacitive Coupling 2500Vrms 1 Channel 8-SOIC	Silicon Labs	SI8271GB-IS
U3	1	Linear Voltage Regulator IC Positive Fixed 1 Output 1.5A DPAK	STMicroelectronics	LD29150DT50R

Dare to innovate differently

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