HALF BRIDGE EVALUATION BOARD

For ICeGaN® P2 Products

USER GUIDE

CGD – UG2404

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CAMBRIDGE GaN DEVICES

Safety Warning

The CGD half bridge evaluation board (EVB) is for evaluation purposes only. It is not intended to be a finished product and does not include all protection features found in a commercial power supply.

DANGER: Do not touch the board when high voltages are applied. There are exposed locations of high voltage on the board when connected to a power source. Brief contact may result in serious injury or death. Allow all components to fully discharge before handling the board. This evaluation board is designed for use by qualified, experienced engineers only. Appropriate safety measures must be put in place before use and the board should never be left unattended.

WARNING: Some components may become hot during operation and remain so afterwards. Operating voltages, currents and temperatures should be monitored closely throughout operation to prevent damage to the board.

CAUTION: This product contains parts susceptible to ESD (electrostatic discharge). ESD prevention procedures must be used while handling the board.



Operating Limits and Recommendations

This evaluation board is for demonstration purposes only and should not be used to power any loads other than an electronic load. Only trained professional using high voltage equipment should operate the board and appropriate safety precautions should be followed.

Heat dissipation

The board has been experimentally verified to be able to dissipate 10 W power loss in the GaN devices at 50 ℃ ambient temperatures. Do not touch the circuit components until the components cool down after turning off. Therefore, it is recommended to use a thermal camera to monitor the circuit temperature during circuit operation and turn off the power if the temperatures rise above nominal operating temperatures.

Target Audience

This guide, along with the board itself, is aimed at experienced engineers and assumes a knowledge of necessary equipment to analyse the performance of the circuit board. It is designed to enable SMPS engineers, design engineers and technicians involved in the development of a system to rapidly assess the performance of CGD's ICeGaN™.

Technical Support

For support, please contact CGD at techsupport@camgandevices.com.

Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial release	HL	14/05/2024
1.1	Update the fan part number in BOM	HL	20/05/2024
2.0	Updated title, clarified some wording around variants	DM	15/04/2026

Contents

TARGET AUDIENCE 3
TECHNICAL SUPPORT 3
REVISION HISTORY 3
1. INTRODUCTION 5
1.1 Block Diagram and Key Features 6
1.2 Connection Guideline 8
2. TEST RESULTS 10
3. SCHEMATIC AND PCB LAYOUT 13
4. BILL OF MATERIALS 18

1. Introduction

The CGD65C025SP2 half-bridge evaluation board is designed for evaluations of CGD65C025SP2's switching performance. Figure 1 shows a picture of the board. The board consists of a half bridge with two CGD65C025SP2 devices along with isolated driver ICs and power supplies. CGD65C025SP2 is a 650-V and 25-mΩ GaN power IC in a bottom-side cooled BHDFN (Bottom Heat-spreader DFN) package, which has enhanced thermal performance and is suitable for high-power applications. The board also includes different terminals, headers, soldering pads, and test points to allow users to easily connect, test, and modify the board.



Figure 1 CGD65C025SP2 half bridge evaluation board.

A heatsink and a 12-V fan are included, as shown in Figure 2, to improve heat dissipation and enable continuous operations at high power. The heatsink and fan are strategically placed on the bottom, allowing the power devices to be positioned on the top. This arrangement facilitates easy monitoring of their case temperature with a thermal camera. Sufficient distance between the fan and test bench should be maintained to ensure enough air flow, which can be achieved by using 80mm standoffs. A plastic washer should be used to ensure sufficient insulation between the standoffs and PCB.

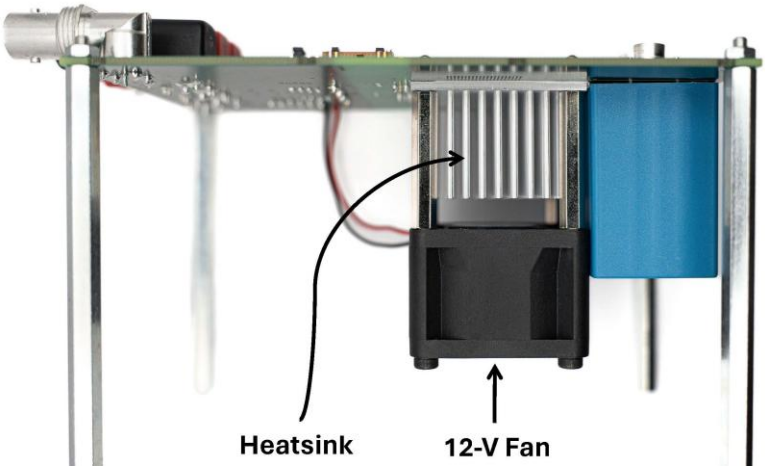


Figure 2 Side view of CGD65C025SP2 half bridge evaluation board.

1.1 Block Diagram and Key Features

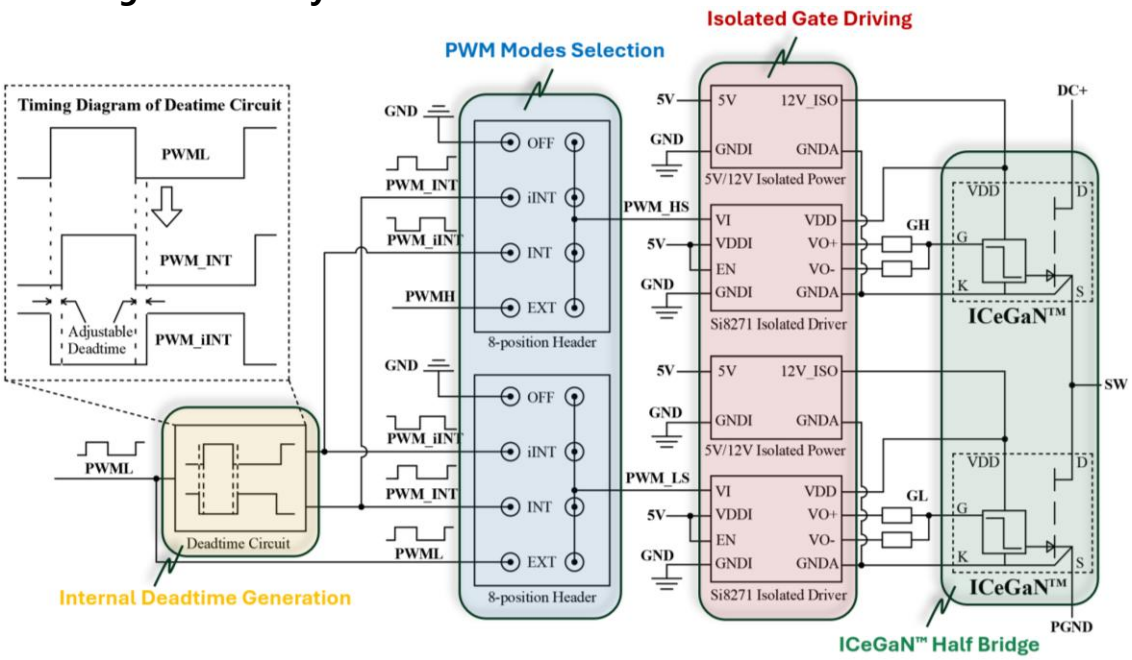


Figure 3 Simplified circuit diagram of CGD65C025SP2 half bridge evaluation board.

A simplified circuit diagram shown in Figure 3 highlights the four functional blocks of the evaluation board:

- **Internal deadtime generation:**
  The deadtime circuit converts PWML into two complementary signals, i.e., PWM_INT and PWM_iINT, and the deadtime can be configured from 0 ~ 250 ns via changing the positions of the header caps. The detailed descriptions of signals in the board can be found in Table 1.

Table 1 Nomenclature of signals.

Signals	Descriptions
GND	The ground for logic and control circuits.
5V	5 V supply voltage for the logic and control circuits.
PWML	The external PWM logic signal to be connected to the low-side gate driver. PWML is connected to one of the BNC connectors.
PWM_LS	The logic input of the low-side gate driver.
PWMH	The external PWM logic signal to be connected to the high-side gate driver. PWMH is connected to one of the BNC connectors
PWM_HS	The logic input of the high-side gate driver.
PWM_INT	The PWM logic signal from the internal deadtime generation circuits. The rising edge of PWML is delayed by the selected deadtime to generate PWM_INT.
PWM_iINT	The PWM logic signal from the internal deadtime generation circuits. PWM_iINT is complementary to PWM_INT and has a deadtime selected by the header cap.
DC+	The positive terminal of the DC bus capacitors.
SW	The switching node of the half bridge.
PGND	The power ground which is isolated to GND.
GL	The gate of the low-side device.
GH	The gate of the high-side device.

- **PWM modes selection:**
  Two 8-position headers are used to provide more flexibility in logic signal connections. Low-side and high-side gate drivers' logic signals, i.e., PWM_LS and PWM_HS, can be connected to ground (OFF mode), external signals (EXT mode), internal signals from the deadtime circuit (INT mode), or swapped internal signals (iINT mode).

Table 2 PWM modes.

PWM modes	Description
OFF	The logic signal to the gate driver is tied to GND.
iINT	The logic signals to high-side and low-side gate drivers are swapped.
INT	The logic signal of the gate driver is from the internal deadtime generation circuits
EXT	The logic signal of the gate driver is from the external signal connected to the BNC connectors.

- **Isolated gate driving:**
  The half bridge and the logic circuits are isolated. The isolated power supplies and isolated gate drivers generate 12-V signals to drive the high-side and low-side ICeGaN. The isolated drivers and isolated power supplies are powered by a single 5-V input, which can be connected using the "5 V" and "GND" banana jacks.
- **ICeGaN half bridge:**
  Two ICeGaN CGD65C025SP2 devices are used in the half bridge. The power loop area is designed to be small to achieve clean switching under high di/dt and dv/dt conditions. Although 12 V is chosen in this design to drive ICeGaN, ICeGaN accepts a wider range of driving voltage and can be driven by 9 ~ 20 V. It should be noted that ICeGaN does not need negative drive gate voltage for turn-off like discrete GaN alternatives. Therefore, no additional circuitry is needed to generate negative voltage.

1.2 Connection Guideline

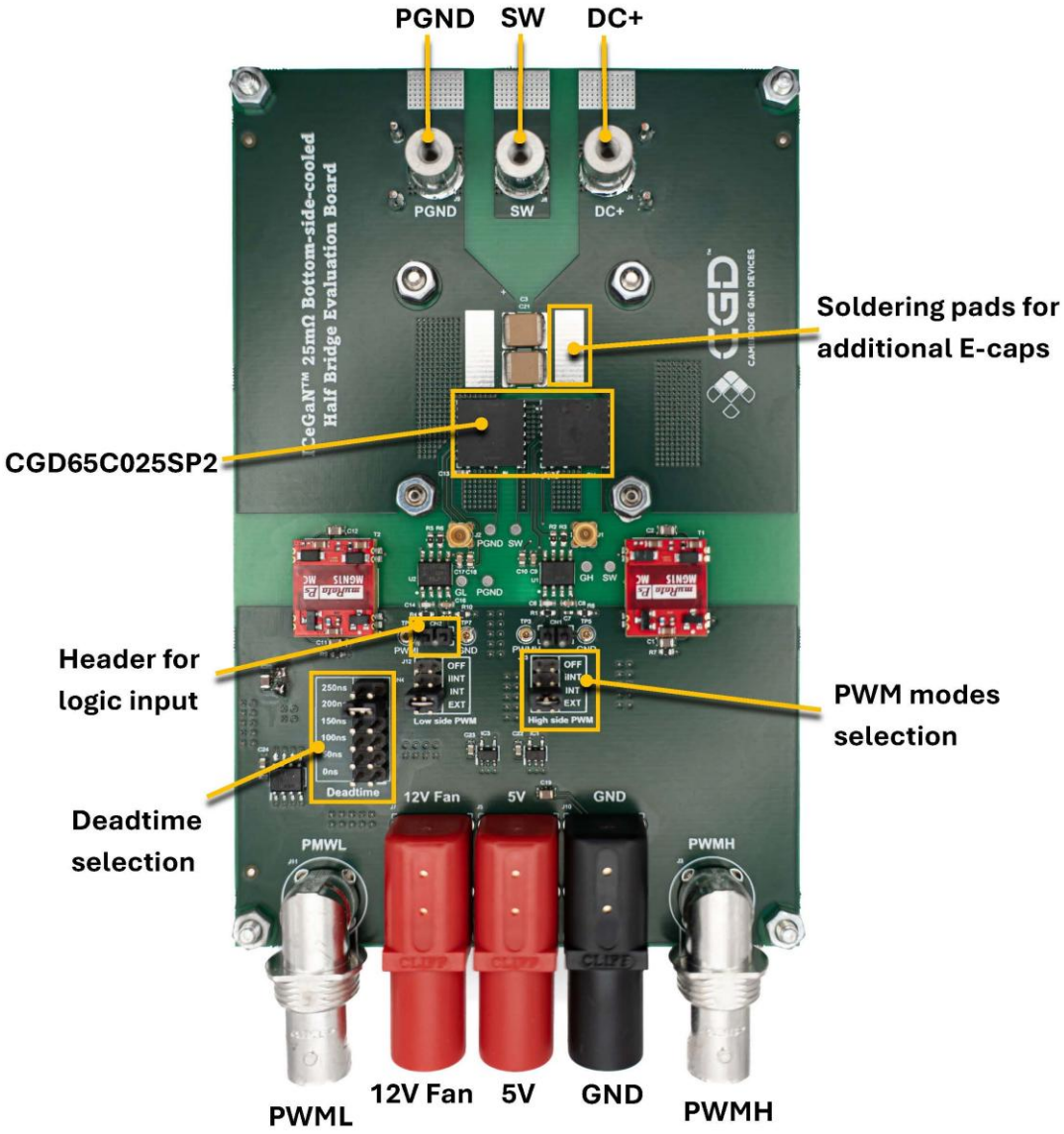


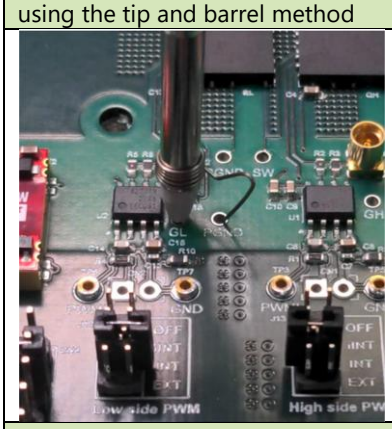
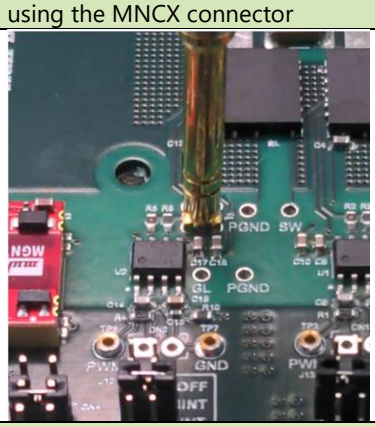
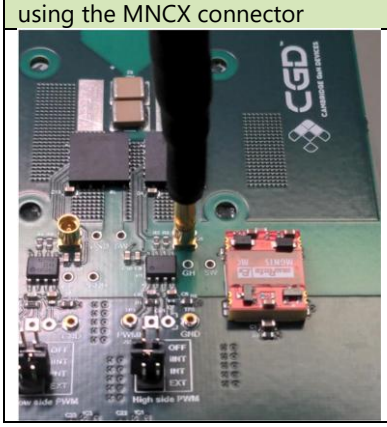
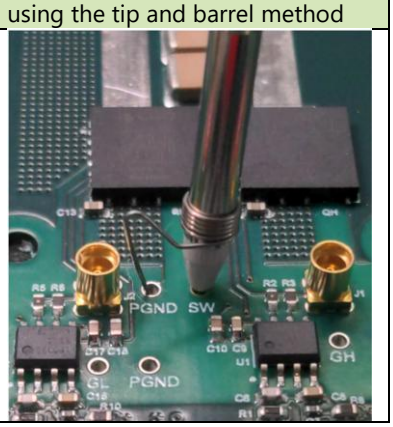
Figure 4 Top view of the board with key connectors and headers highlighted.

Figure 4 highlights the locations of connectors. The guideline for connections is as described below:

- **Half-bridge connection:**
  The power cables can be connected by either soldering wires to the soldering pads or tightening crimp lugs to the cylindrical terminals with M3 bolt. In applications such as AC/DC conversion, there may be a need to increase the buffer capacitance to reduce the ripple. To address this need, two soldering pads were placed next to the ceramic capacitors for soldering additional capacitors.
- **Logic connection:**
  The logic signals to the gate driver may be generated by a function generator or a microcontroller. The BNC connectors can be used to terminate the logic signal when a function generator is used. When a microcontroller is used, the logic signal can be connected to the 2-pin header near the gate driver with jumper wires.

- **Header connection:**
  There is a 12-position header to adjust the deadtime of the internal PWM signals. It is recommended to start with the highest deadtime, i.e., 250 ns, to minimize the risk of a shoot-through event. Then, the deadtime can be gradually reduced to optimize the efficiency. There are two 8-position headers to select the PWM mode via the header caps. It must be **avoided** to set one header to INT mode and another to iINT mode, which will lead to a shoot-through event and damage the devices.
- **Power supply connection:**
  5 V must be provided externally to power the board driving circuitry. All the auxiliary power in the board is supplied by a single 5-V input, which is connected to a banana plug on the bottom as shown in Figure 4. The 12-V fan can be connected if better cooling is required, and the fan shares a common ground with the 5-V signal.
- **Test point connection:**
  The location of different test points as well as the recommendation to contact the test points are summarized in Table 3. The measurement loop area should be kept small to reduce noise couplings. It is recommended to use the MNCX connector to measure the gate signals, because of its better shielding and smaller loop area than the tip and barrel method. It is important to note that a high voltage probe must be used to measure the switching node voltage which switches between 0-V and the voltage applied in DC+. A differential probe or an isolated probe must be used to measure the high-side signals to avoid shorting the switching node with power ground.

Table 3 Recommended probing for different test points.

Low-side gate signal probing using the tip and barrel method	Low-side gate signal probing using the MNCX connector
	
High-side gate signal probing using the MNCX connector	**Switching-node voltage probing using the tip and barrel method**
	

2. Test Results

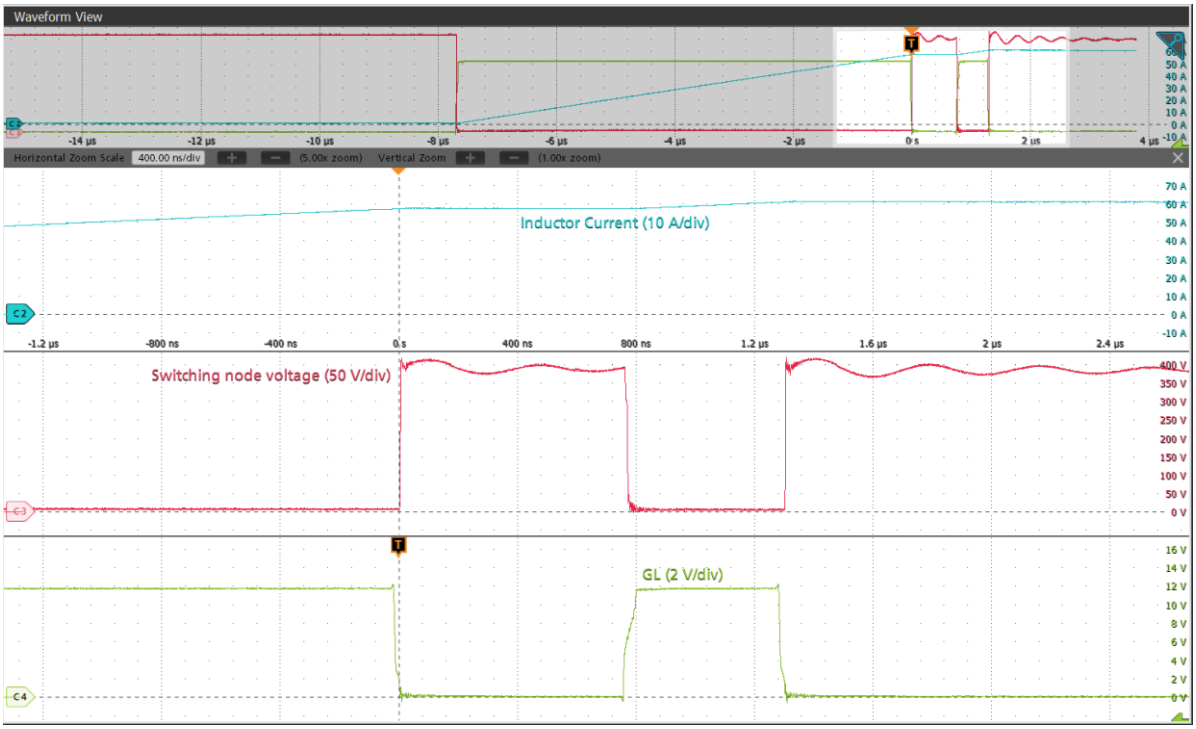


Figure 5 Double pulse test waveform under 60-A hard switching on. The overshoot of switching node voltage is around 20 V.

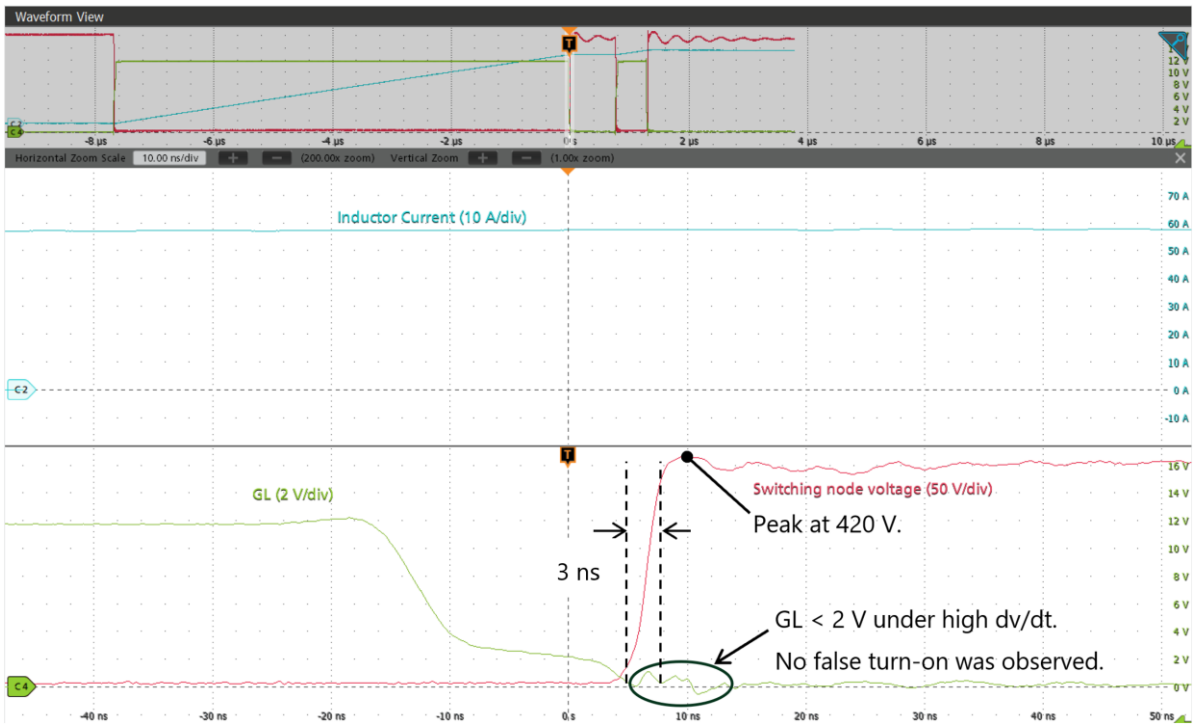


Figure 6 Zoomed-in waveforms under 60-A 400-V hard turn-off.

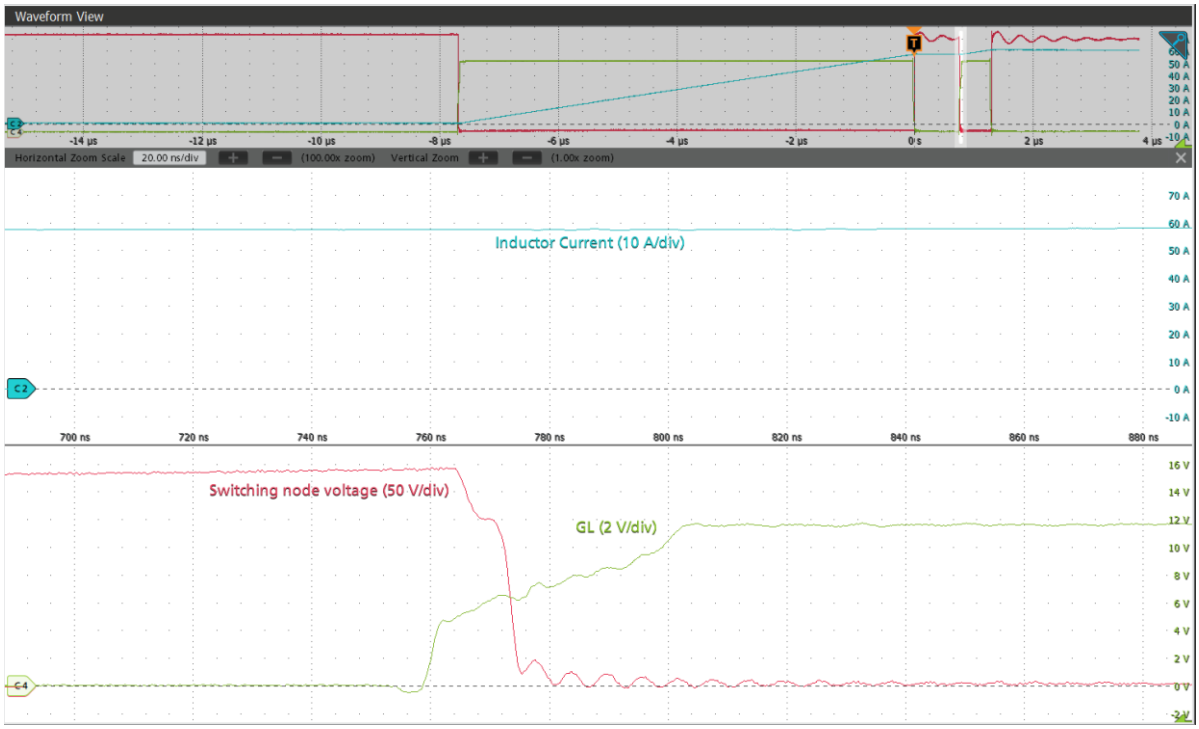


Figure 7 Zoomed-in waveforms under 60-A 400-V hard turn-on.

The waveforms from a double pulse test are displayed in Figure 5. The gate driving signal is clean and has no ringing. The switching node voltage contains small ripple, whose amplitude is around 20V. The DC bus capacitance can be increased if smaller ripple is needed. Zoomed-in waveforms under 60-A 400-V hard turn-off and turn-on are shown in Figure 6 and Figure 7, respectively. The gate-source voltage was below the 2-V threshold voltage under a ~ 130 V/ns dv/dt condition, indicating that there was no false turn under high dv/dt. The peak of the switching node voltage is around 420V.

The board was also tested continuously at 1 kW as a synchronous buck converter. The test conditions are summarized in Table 4. The waveforms of buck operations are shown in Figure 8. The gate-source and drain-source signals are clean and don't have unexpected oscillations.

Table 4 Test conditions of the synchronous buck converter.

Parameter	Value
Input voltage	400 V
Switching frequency	100 kHz
Duty cycle	50 %
Deadtime	200 ns
Ambient temperature	21 ℃
Output power	1 kW

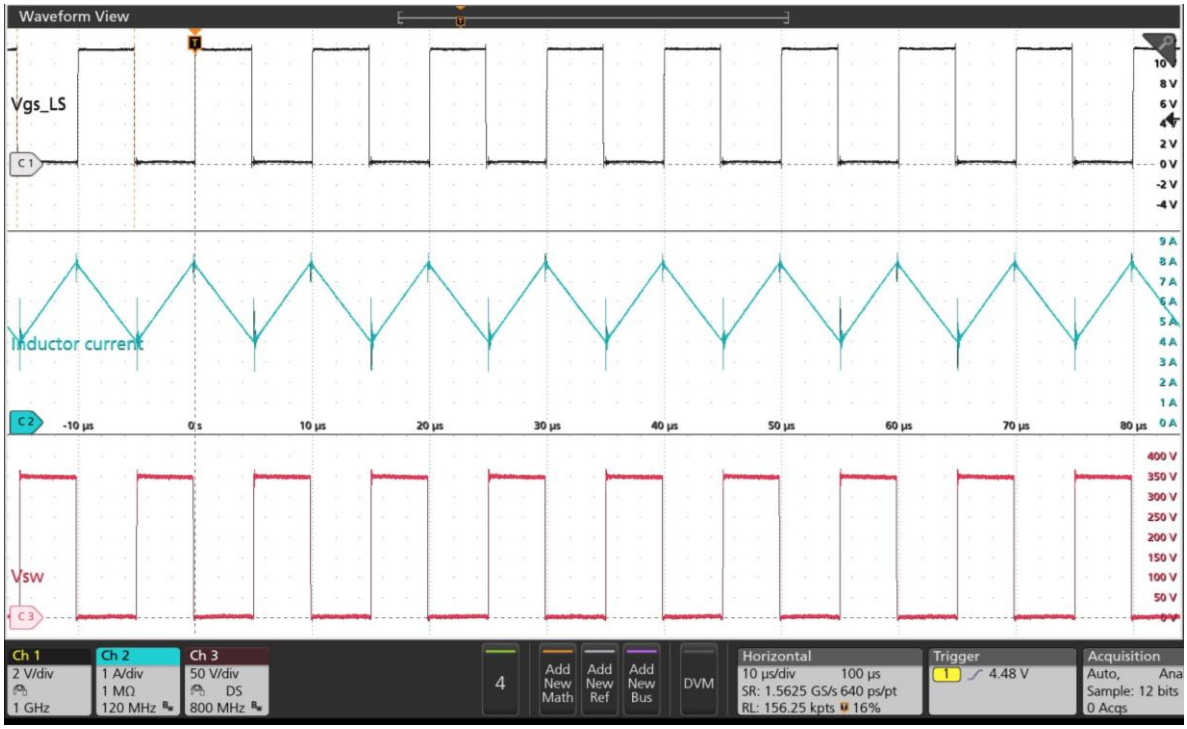


Figure 8 Continuous operating waveforms as a 1 kW synchronous buck converter. The switching frequency is 100 kHz and the duty cycle is 0.5.

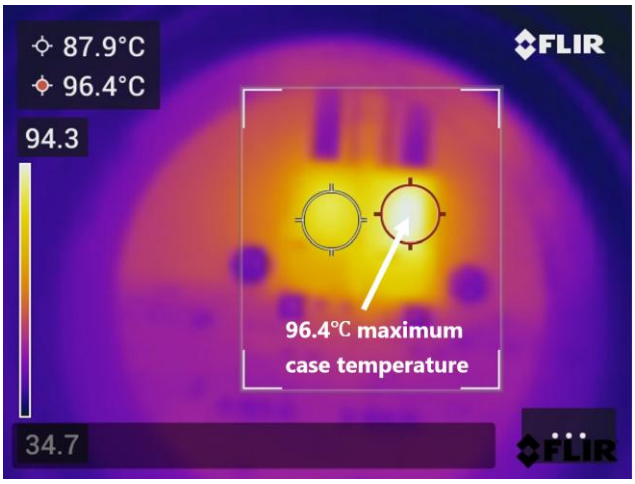


Figure 9 Thermal performance under 10 W power loss. The board is placed inside a 50 ℃ thermal chamber. The maximum case temperature of the devices is 96.4 ℃.

The thermal performance was checked by running the board at 10 W power loss inside a 50 ℃ thermal chamber. The maximum case temperature was measured to be 96.4 ℃ at steady state, as shown in Figure 9.

3. Schematic and PCB Layout

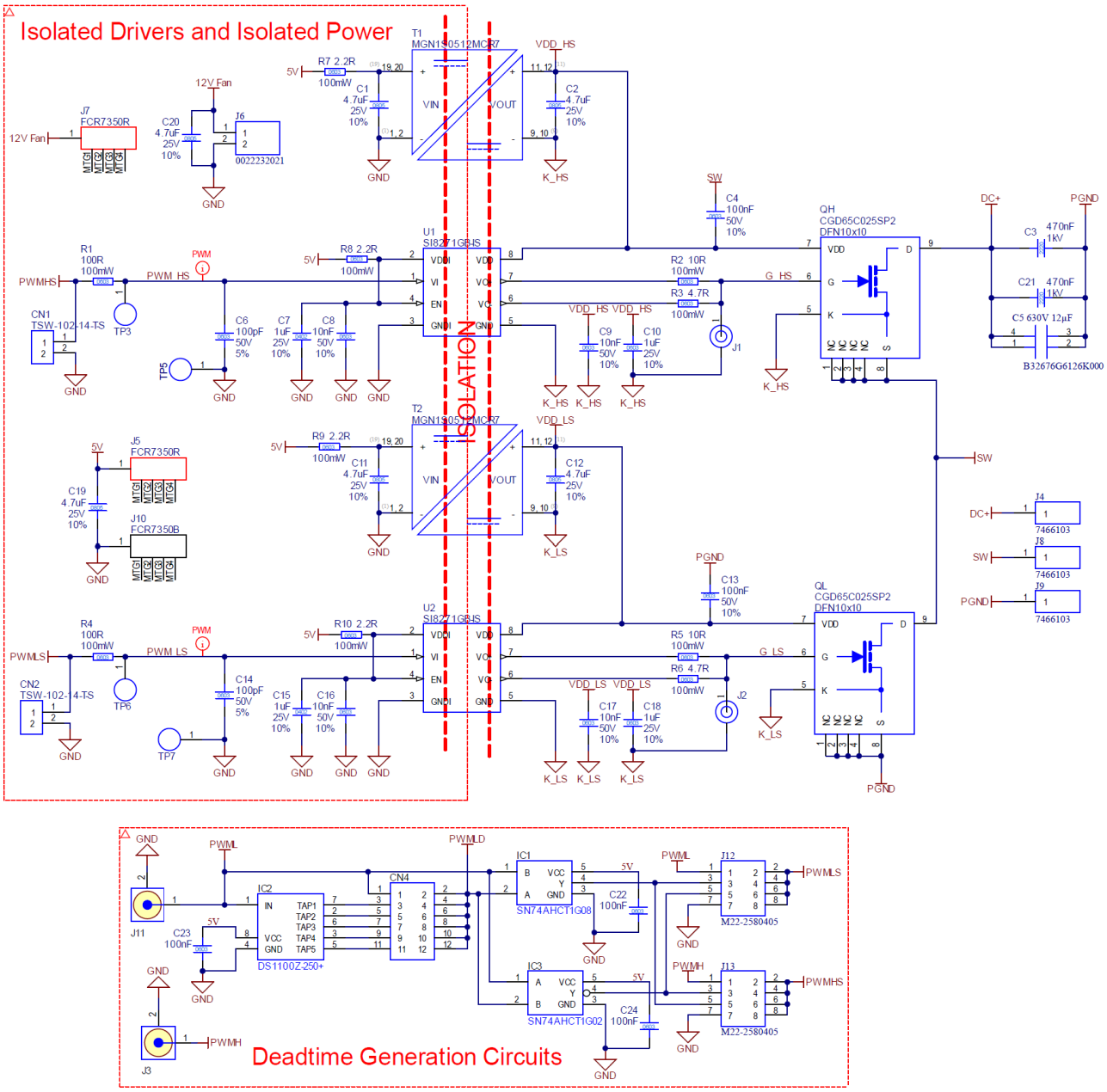


Figure 10 Schematic of the half-bridge evaluation board.

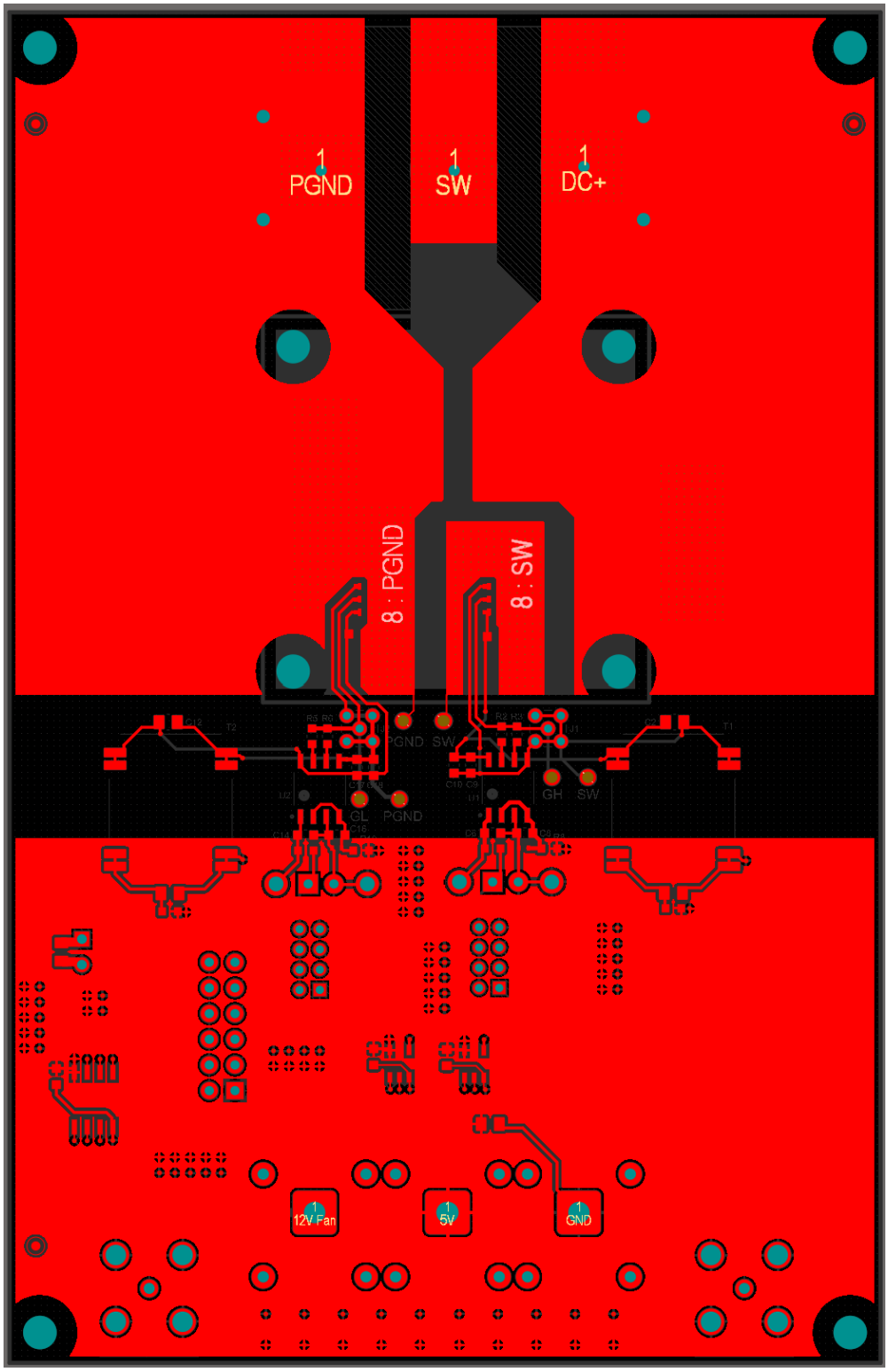


Figure 11 PCB layout of the first layer.

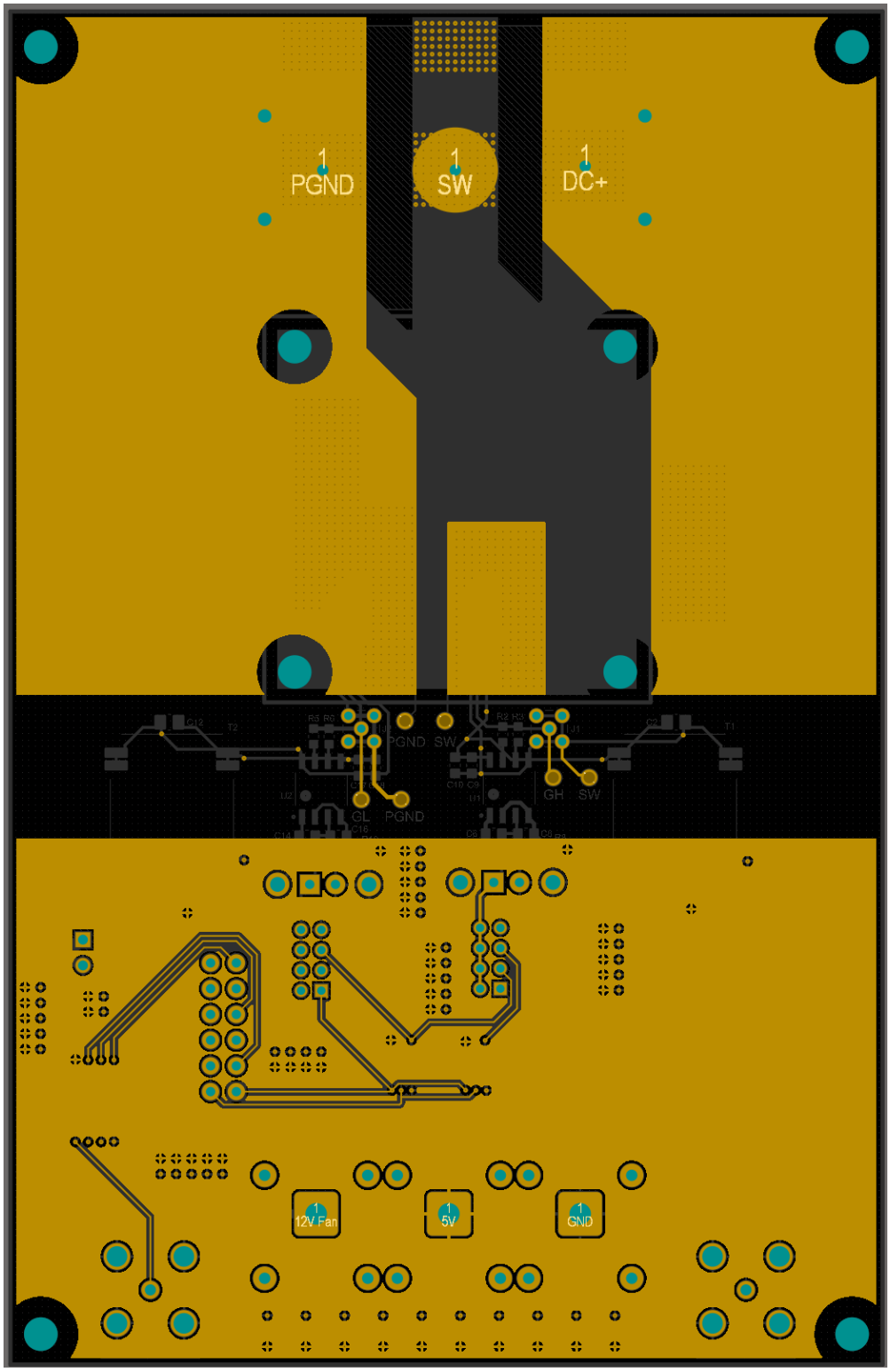


Figure 12 PCB layout of the second layer.

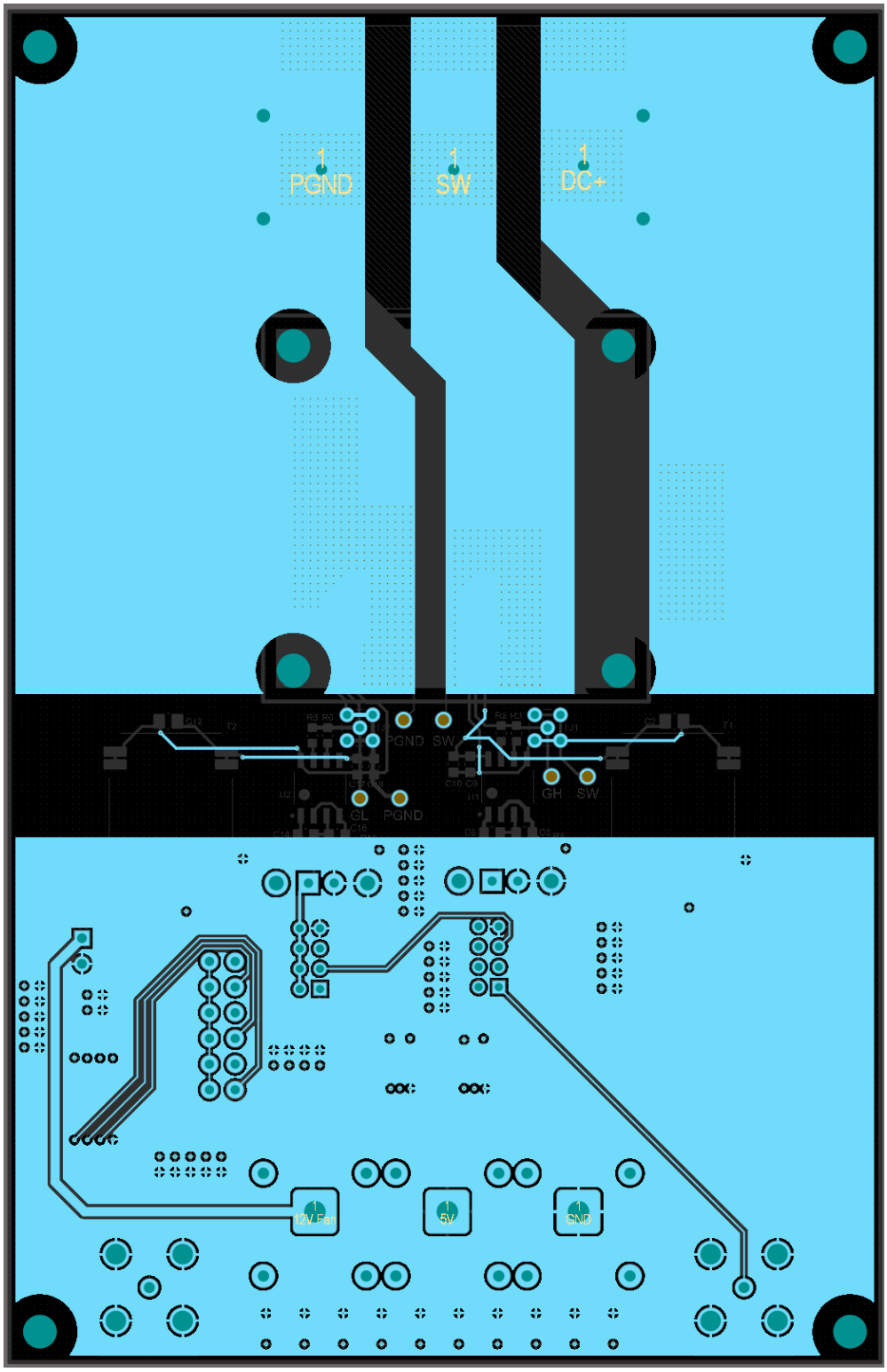


Figure 13 PCB layout of the third layer.

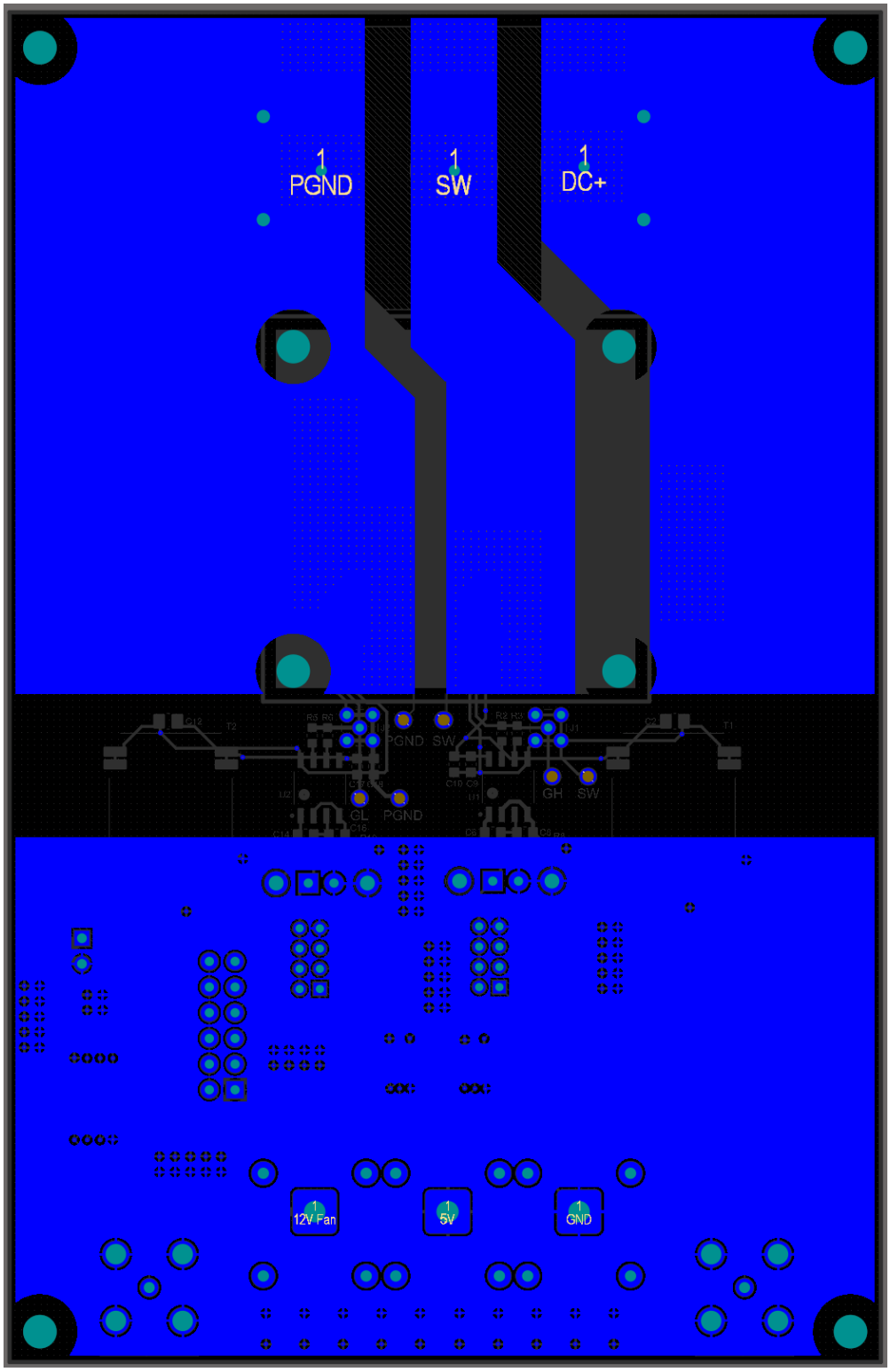


Figure 14 PCB layout of the fourth layer.

4. Bill of Materials

Table 5 Bill of materials of the evaluation board.

Designator	QTY	Description	Part Number	Manufacturer
C1, C2, C11, C12, C19, C20	6	4.7 µF ±10% 25V Ceramic Capacitor X7R 0805 (2012 Metric)	CC0805KKX7R8BB475	YAGEO
C3, C21	2	0.47 µF ±10% 1000V Ceramic Capacitor X7R 2220 (5750 Metric)	2220Y1K00474KXRWS2	Knowles Syfer
C4, C13, C22, C23, C24	5	0.1 µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C0603C104J1RACTU	KEMET
C5	1	12 µF Film Capacitor 630V Polypropylene (PP), Metallized Radial	B32676G6126K000	TDK
C6, C14	2	100 pF ±5% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	CC0603KRX7R9BB101	YAGEO
C7, C15	2	1 µF ±10% 25V Ceramic Capacitor X5R 0402 (1005 Metric)	C1005X5R1E105K050BC	TDK
C8, C9, C16, C17	4	10000 pF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	CC0603KRX7R9BB103	YAGEO
C10, C18	2	1 µF ±10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	CC0603KRX7R8BB104	YAGEO
CN1, CN2	1	Connector Header Through Hole 2 position 0.100" (2.54mm)	TSW-102-14-T-S	Samtec Inc.
CN4	1	Conn Unshrouded Header HDR 12 POS 2.54mm Solder ST Thru-Hole Bag	M20-9980645	Harwin
IC1	1	Single 2-input, 4.5-V to 5.5-V AND gate with TTL-compatible CMOS inputs 5-SOT-23 -40 to 125	SN74AHCT1G08DBVT	TI
IC2	1	DS1100 Series 5.25 V 250 ns Surface Mount 5-Tap Economy Timing Element - SOIC-8	DS1100Z-250+	Analog Devices
IC3	1	Single 2-input, 4.5-V to 5.5-V NOR gate with TTL-compatible CMOS inputs 5-SOT-23 -40 to 85	SN74AHCT1G02DBVT	TI
J1, J2	2	RF Connectors / Coaxial Connectors MINI PUSH-ON CONN RECEPT STR	MMCX-R-PC(40)	Hirose
J3, J11	2	Right Angle 50Ohm Thru Hole Bulkhead Fitting BNC Conn; jack; Solder Term Nickel	5415025-1	TE Connectivity
J4, J8, J9	3	1 Pin Screw Terminal, Power Tap M3 Surface Mount	7466103	Wurth Elektronik
J5, J7	2	Banana Jack Connector Standard Banana Solder Red	FCR7350R	CLIFF
J6	1	Connector Header Through Hole 2 position 0.100" (2.54mm)	0022232021	Molex
J10	1	Banana Jack Connector Standard Banana Solder Black	FCR7350B	CLIFF
J12, J13	2	Connector Header Through Hole 8 position 0.079" (2.00mm)	M22-2580405	Harwin
QH, QL	2	25 mΩ 650V 60A Bottom-side-cooled ICeGaN	CGD65C025SP2	CGD

R1, R4	2	100 Ohms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric)	RC0603FR-07100RL	YAGEO
R2, R5	2	10 Ohms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric)	560112116013	Wurth Elektronik
R3, R6	2	4.7 Ohms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric)	CRT0805-BY-4R70ELF	Bourns
R7, R8, R9, R10	4	2.2 Ohms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric)	CRCW06032R20FNEA	Vishay
T1, T2	2	Isolated Module DC DC Converter 1 Output 12V 83.3mA 4.5V - 5.5V Input	MGN1S0512MC-R7	Murata
TP3, TP5, TP6, TP7	4	Test Point 0.64mm - 0.94mm pin receptacle	7305-0-15-15-47-27-10-0	Mill-Max
U1, U2	2	4A Gate Driver Capacitive Coupling 2500Vrms 1 Channel 8-SOIC	SI8271GB-IS	Skyworks
Heatsink	1	38.1 x 38.1 Aluminum Heatsink with 4 M3 Holes	3-151510US79776	Cool Innovation
Fan	1	Sunon Axial Fan, 12 V DC, DC Operation, 10.8 CFM, 960mW, 92mA Max, IP20, 40 x 40 x 20mm	MF40201VX-1000U-F99	Sunon Fans

Dare to innovate differently

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