HALF BRIDGE EVALUATION BOARD FOR H1 AND H2 ICEGAN®

User Guide

CGD-UG2202

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COMPANY CONFIDENTIAL

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CAMBRIDGE GaN DEVICES

Safety Warning

DANGER: Do not touch the board when high voltages are applied. There are exposed locations of high voltage on the board when connected to a power source. Brief contact may result in serious injury or death. Allow all components to fully discharge before handling the board. This evaluation kit is designed for use by qualified, experienced engineers only. Appropriate safety measures must be put in place before use and the board should never be left unattended.

WARNING: Some components may become hot during operation and remain so afterwards. There is no built in electrical or thermal protection. Operating voltages, currents and temperatures should be monitored closely throughout operation to prevent damage to the board.

CAUTION: This product contains parts susceptible to ESD (electrostatic discharge). ESD prevention procedures must be used while handling the board.



Operating Limits and Recommendations

Operating outside this window is not recommended and may cause damage.

Voltage limits

CGD has a recommended maximum operation of 650 V on the Half Bridge (HB) evaluation board.
PWM inputs should not exceed 5.5 V as this can damage the drivers and deadtime circuitry. CGD ICeGaN™ (Gate and VDD) is only rated between the voltages of 9 and 20 V. Operating outside of this range will damage the HEMTs.

Heat dissipation

Heatsinking the GaN switch devices has been provided through bottom side cooling of the devices. An electrically insulating thermal interface material (TIM) is provided between the exposed copper of the PCB and the heatsink. The heatsink itself has an Rth of 3.5 K/W. CGD makes no guarantees as to the thermal performance of the heatsinking solution provided.

Start up

It is highly recommended to apply the low voltage inputs, specifically the 18 V supply, prior to the application of high voltage inputs.

User Guide Overview

This user guide will highlight the capabilities of the half bridge evaluation board to enable the customer to adapt the board into a topology of their choosing and assess the performance of CGD 650 V GaN HEMTs. Further, this user guide will show how CGD ICeGaN enables enhancement mode GaN to be driven as though it is a MOSFET, an industry first. CGD ICeGaN accepts voltages of 9-20 V rather than the 5-6 V typically accepted by e-GaN. Further ICeGaN increased the threshold of the device from ~1.3 V for e-GaN to around 3V.

Target Audience

This guide, along with the board itself, is aimed at experienced engineers and assumes a knowledge of necessary equipment to analyse the performance of the board. It is designed to enable SMPS engineers, Design Engineers and Technicians involved in the development of a system to rapidly assess the performance of CGD ICeGaN within their desired topology.

Technical Support

CGD is happy to provide expert help with any questions or problems. For support, please contact CGD at techsupport@camgandevices.com.

Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	JF	10/03/2022
2.0	Updated H2 Series and Section 6 figures	MC	23/08/2023
3.0	Updated part numbers in section 1	DM	22/08/2025
4.0	Updated Title for clarity	DM	26/02/2026

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FIGURE LIST 27

1 Board Overview

Assembly Name	CGD Devices Utilised	$R_{DS(on)}$	Capabilities	Device Package
CGD-ASYEVB02501-01	CGD65A055SH2	55 mΩ	ICeGaN	DFN8x8
CGD-ASYEVB02301-01	CGD65A130SH2	130 mΩ	ICeGaN	DFN8x8
CGD-ASYEVB02201-01	CGD65B130SH2	130 mΩ	ICeGaN	DFN5x6
CGD-ASYEVB01601-01	CGD65B240SH2	240 mΩ	ICeGaN	DFN5x6

Table 1 - Different Board Variations Covered by this User Guide

The Cambridge GaN Devices (CGD) Half Bridge Evaluation Board demonstrates the performance advantages of CGD GaN over its competitors through ICeGaN Technology. CGD ICeGaN Gate enables the driving of GaN HEMTs through an extremely large range of 9 to 20 V. This allows for easy and affordable drive through readily available silicon drivers, without having a detrimental impact on GaN's excellent switching performance. In addition, CGD's ICeGaN increases the threshold voltage of the GaN to around 3 V, which prevents unwanted turn-on events and eliminates the need for negative driving voltages, as required for other discrete enhancement mode HEMTs currently available on the market.

The evaluation board consists of two 650 V GaN HEMTs with same $R_{DS(on)}$ and same package configured as a half-bridge, and variable gate drive voltage from 9 V to 20 V. This user guide is applicable for all device types, but it is worth noting the 240 mΩ, 200 mΩ and 130 mΩ parts are available a DFN 5x6 while the 55 mΩ and 130 mΩ are available in the DFN 8x8 package. All board functionality is identical and so no distinction will be made between the two different PCBs for the remainder of this user guide. (With the exception of the Schematic and Layout captures in Chapter 6.)

Please note: While this board has a current sense observation pin available, CGD does not recommend its use as the current sensing requires additional circuitry to operate as designed not implemented on this evaluation board.

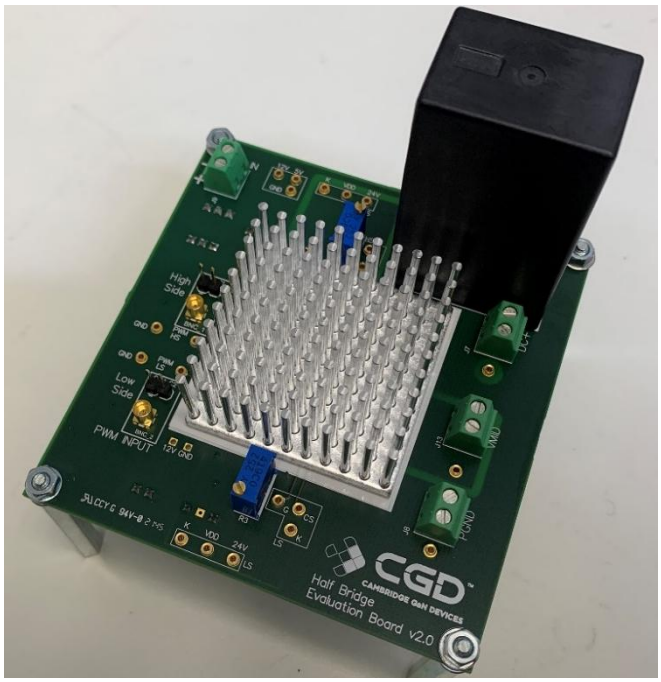

Figure 1 - Photograph of Half Bridge Evaluation Board

1.1 Feature List

- 2 x 650 V CGD Enhancement Mode GaN HEMTs with ICeGaN Gate

- 2 x Silicon Labs SI8271AB-IS Isolated Gate Driver (1 per side), adjustable drive amplitude 9-20 V

1.2 Minimum Required Equipment

- High Voltage Supply
- Low Voltage Supply (18 V, approx. 400 mA)
- Controller/Waveform Generator
- Application Dependent Load
- Oscilloscope (Including Required Voltage-Rated Probes)

1.3 Inputs and Outputs

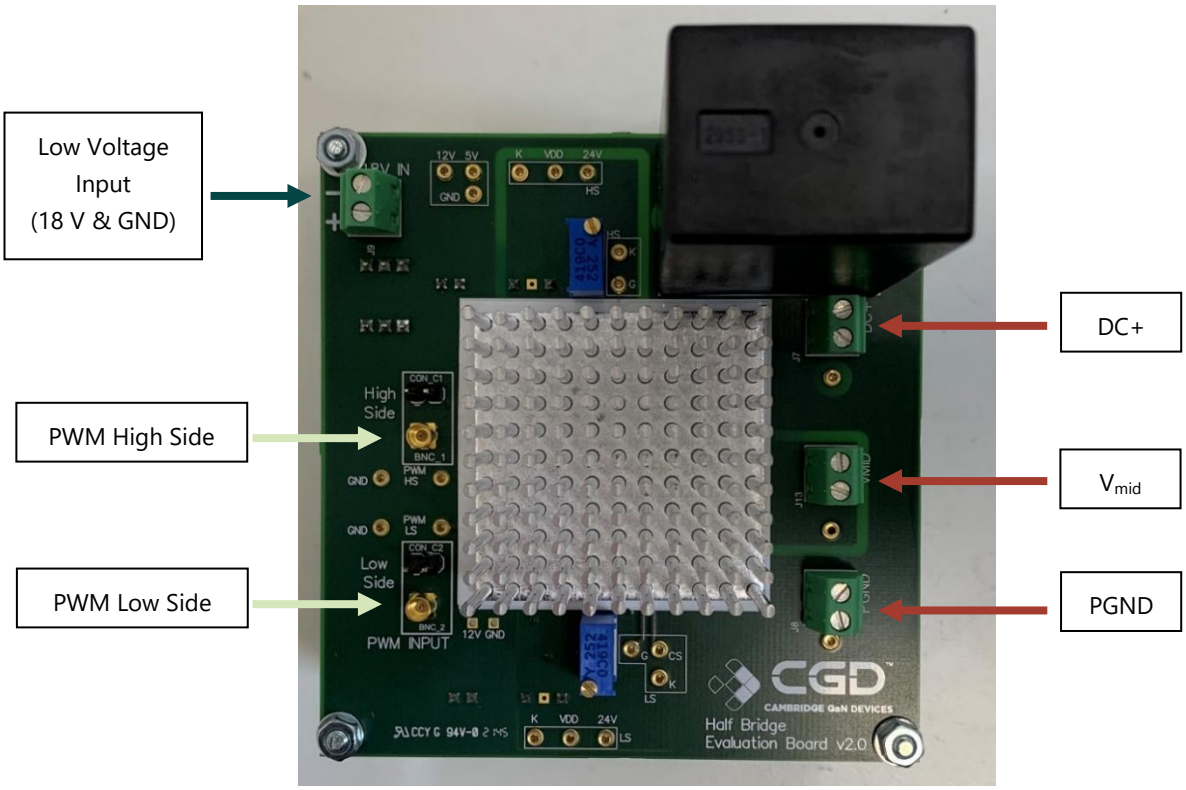

Figure 2 - Photograph of Half Bridge Board Showing Inputs and Outputs

The half bridge board does not provide any galvanic isolation between high voltage ground (PGND) and signal ground (GND). All signal inputs are common to GND.

Signal	Ports	Comments
DC+	Terminal Block	Max 650 V.
PGND	Terminal Block	0V of the Half Bridge Board. Return path of DC+.
V_{mid}	Terminal Block	Mid-point of the Half Bridge.
18 V	Terminal Block	DC Supply Input for all Low Voltage Gate Driver Circuits. Max 20 V.
GND	Terminal Block	Return path for 18 V DC input. Terminal block shared with 18 V.
PWM HS	MMCX 50Ω Coax & Pin Header	High side gate drive input.
PWM LS	MMCX 50Ω Coax & Pin Header	Low side gate drive input.

Table 2 - Evaluation Board Inputs and Outputs

1.4 CGD GaN Half Bridge Overview

The illustration below shows simplified schematics for the half bridge evaluation board, highlighting the variable gate voltage drive. Note how the 9-20 V is delivered both to the CGD device and the Silicon Labs driver. This means V_{DD} voltage on the CGD device matches the on-state gate voltage. This board does not support decoupling these voltages.

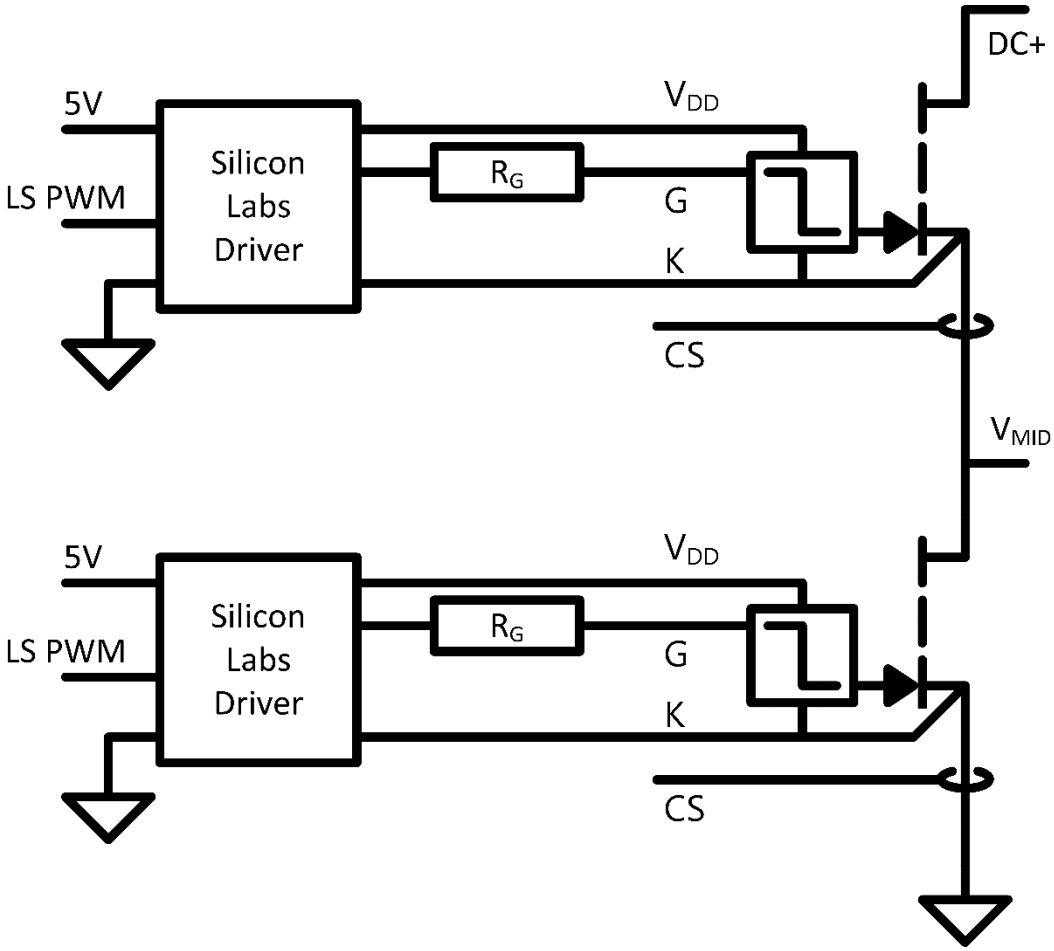

Figure 3 - Simplified Schematic of HB Evaluation Board Showing Gate Drive

1.5 Decoupling Capacitors

For purposes of signal quality, a large DC film capacitor of 18 µF and a local ceramic capacitor of value 1 uF have been included on the PCB. It is recommended to leave these in place through any testing to prevent any low frequency ringing on the DC rail. Both capacitors are rated >700 V_{DC} to allow testing of the CGD device up to its rated 650 V.

1.6 Probe Locations

Below in Figure 4 is a photograph of the half bridge board with probe locations labelled. All probe points on the board are labelled, and probe locations marked "K" is the 'Kelvin' reference relative to the other pins contained within its box.

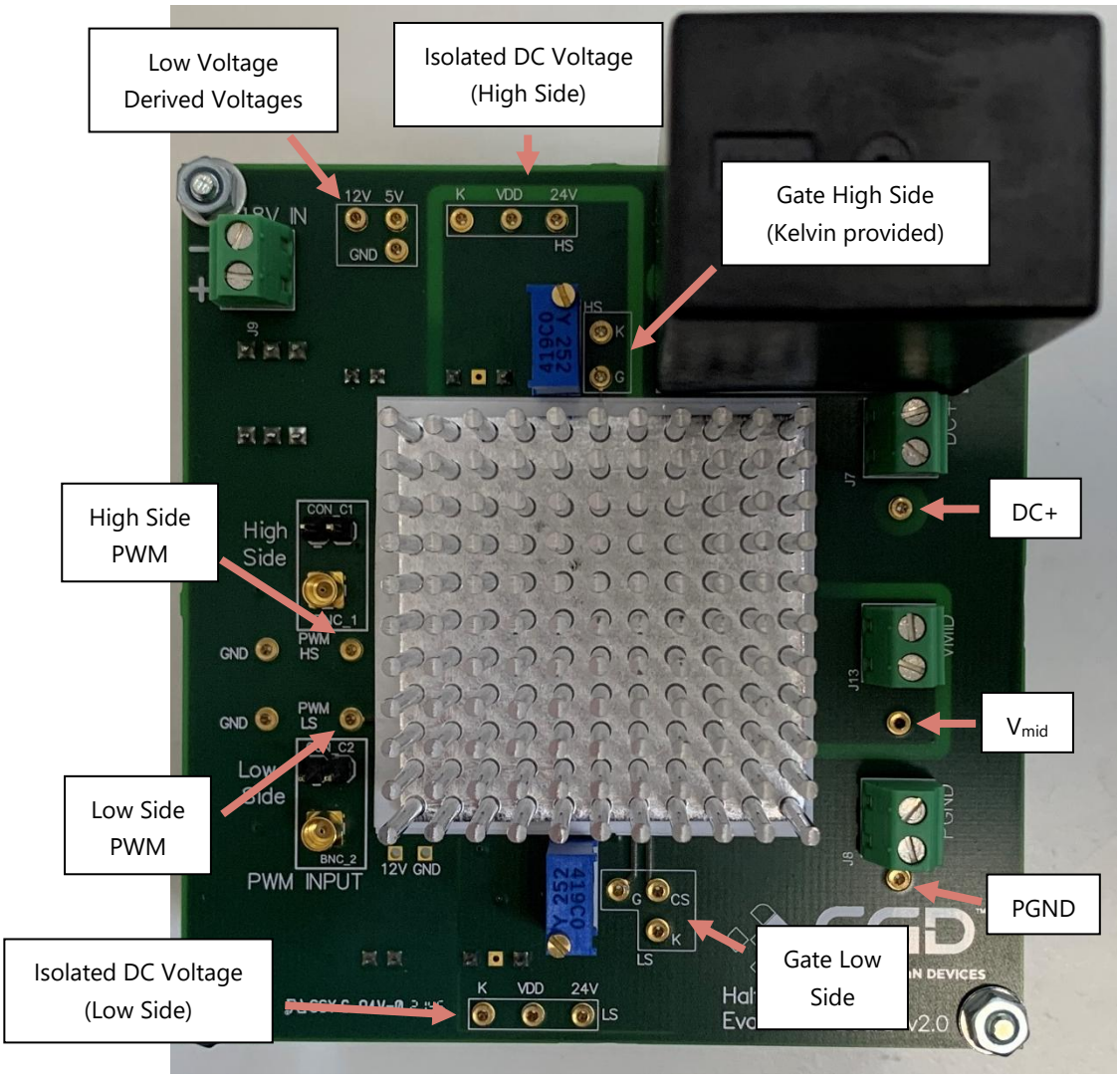

Figure 4 - Photograph of HB Evaluation Board Highlighting Test Pin Locations for Scope Probes

1.7 Heatsinking

The half bridge evaluation board comes with a heatsink attached through an adhesive electrically isolating thermal interface material. The CGD devices included on the half bridge evaluation board are all bottom side cooled and an exposed copper area can be found on the top of the PCB for heat extraction through this heatsink. The heatsink itself has an RTH of 3.5 K/W. CGD makes no guarantee as to the thermal performance of the HB evaluation board and recommends the user observes the board at all times while testing with a thermal camera. A 12 V and GND pair of connections have been provided near the heatsink for the user to attach an actively cooled heatsink if the testing circuit requires this.

2 Variable Drive Voltage

To fully demonstrate the capabilities of CGD ICeGaN, variable voltage gate drive has been included on the HB evaluation board. The Silicon Labs Isolated Driver enables excellent performance whilst allowing easy adjustment between 9 V and 20 V drive.

The Silicon Labs gate driver has the same operation for both the high side and the low side. All consequent remarks in this section are applicable to both high side and low side, therefore, this user guide will not distinguish between them. A representative schematic for each Silicon Labs driver voltage generation is shown below. Independent supplies are provided for low side and high side drive. The isolated ground is referred to in the following diagram as "kelvin". The kelvin contact is connected directly to the source of the GaN transistor inside the package to reduce voltage drop as a result of current through the source pins.

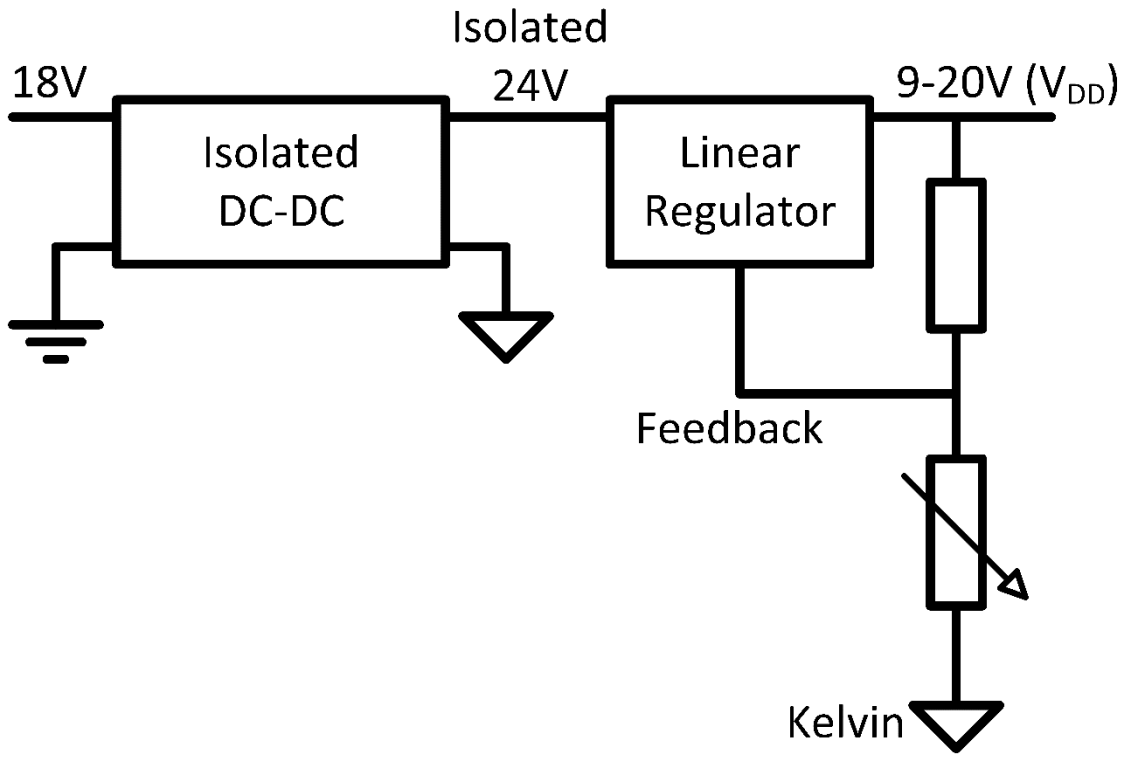

Figure 5 - Basic Schematic Showing V_{DD} Generation

Adjusting the variable resistor (R3 on low side and R26 on the high side) enables the feedback of the linear regulator to be adjusted such that VDD can vary over the rated range for ICeGaN of 9-20 V. It is possible that variations in the resistor values could enable VDD outside this range – exceeding the rated range is not recommended. It is recommended that any adjustment to VDD is performed with high voltage disconnected, and the PWM inputs turned off, to prevent any damage to the HEMTs. Test pins labelled "24V", "VDD" and "K" have been included on the board, one set for high side, one for low side, to allow for the monitoring of this voltage as the variable resistor is adjusted. Further note, that the VDD of the high side and low side can be set at different voltages provided both are within the 9-20 V range relative to their kelvin connection.

3 Jumper Selection Options

Below is a picture of the board with the jumpers highlighted. CGD has allowed for drive either through the MMCX input or through the provided header pin. J1 selects between the two for the high side device, and J2 selects between them for the low side device. Observation of the PWM signal delivered to the device is available from the test pins labelled “PWM HS” and “PWM LS”. A ground pin is alongside each probe point.

To select operation from the header, the user should place the jumper in the upper location for both J1 and J2 as photographed below. If the user wishes to use the MMCX connector the user should place the jumper in the bottom position as photographed for both J1 and J2.

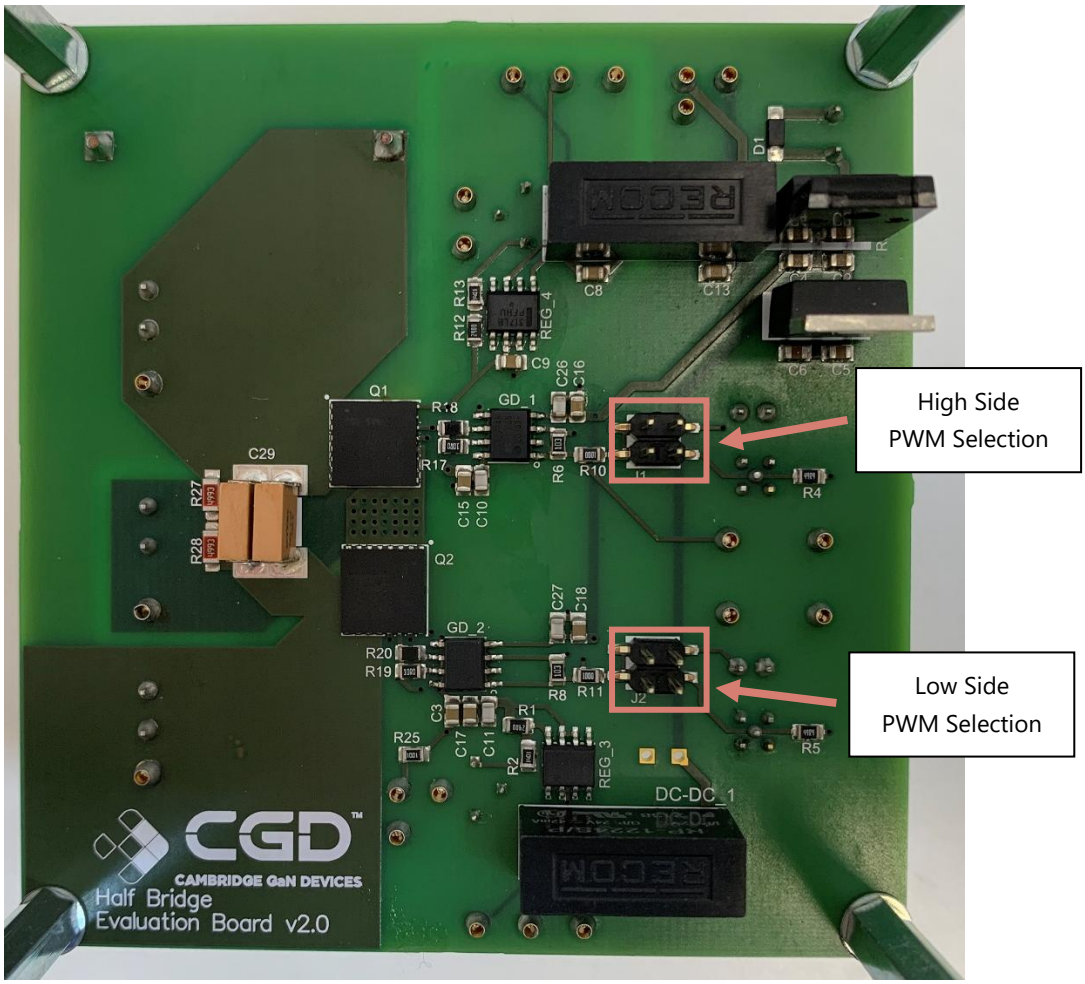

Figure 6 - Photograph of Half Bridge Evaluation Board Underside Showing Jumper Options

4 Example Double Pulse

The output of a double pulse test conducted on the half bridge board is shown below. The board shown is CGD-ASYEVB00801-01. In this example, the low side device is switched. The high side device is briefly switched on during the low side off period to reduce stress on the high side device. Switching conditions are 400 V, 5 A, and a 125 µH inductor was used.

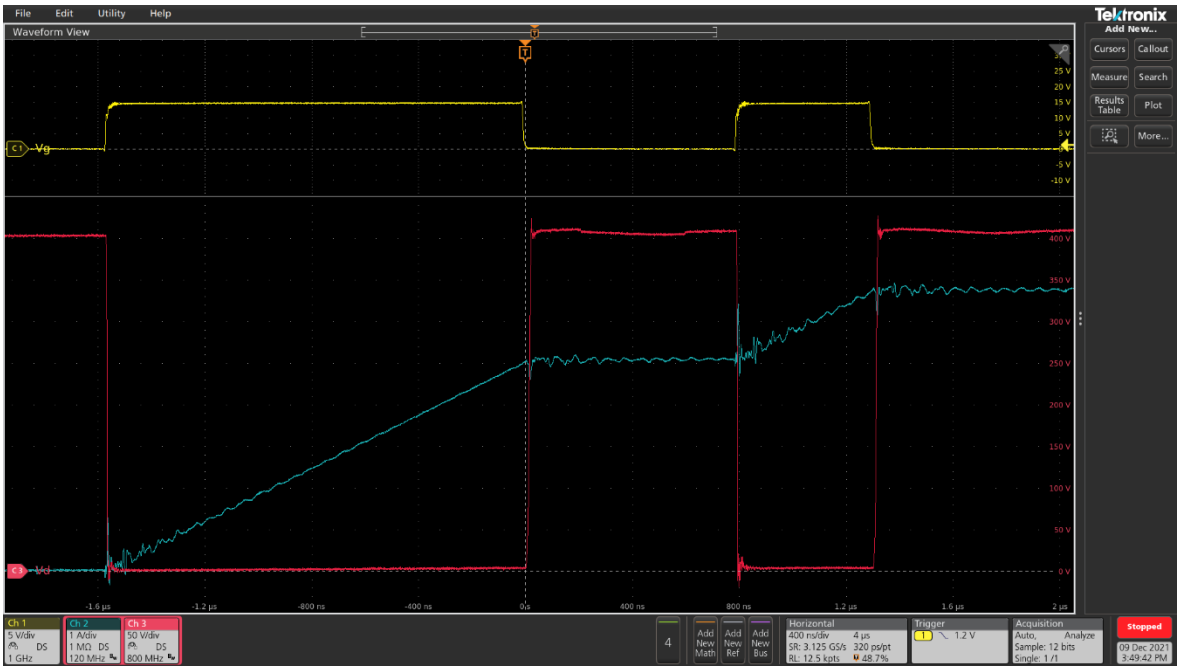

Figure 7 - Capture of 400 V, 5 A Double Pulse Test. (400 ns/div)

Red – V_{mid} 50 V/div, Yellow – Low Side Gate 5 V/div, Blue - Inductor Current 1 A/div

Test Conditions

- 400 V, 5 A low side switching test with 125 µH inductor.
- Half bridge board contained CGD65A130S2.
- Silicon Labs Drivers used at 15 V V_G
- Probes (see Figure 11 for photograph)
  - Gate: low side 'G' pin to 'K' pin (TPP1000) — CH1 - Yellow
  - Current: inductive probe around inductor lead (TCP0030A) — CH2 - Blue
  - V_{mid}: 'Vmid' pin to 'PGND' pin (TPP0850) — CH3 - Red

Results

Note these results were extracted from the csv output of the waveforms and are limited in their accuracy by the sampling rate of the scope.

- V_{mid} Rise
  - 10%-90% Rise Time: 11.2 ns
  - dv/dt: 29 V/ns (average between 10 and 90%)
- V_{mid} Fall
  - 10%-90% Fall Time: 3.4 ns
  - dv/dt: -94 V/ns (average between 10 and 90%)

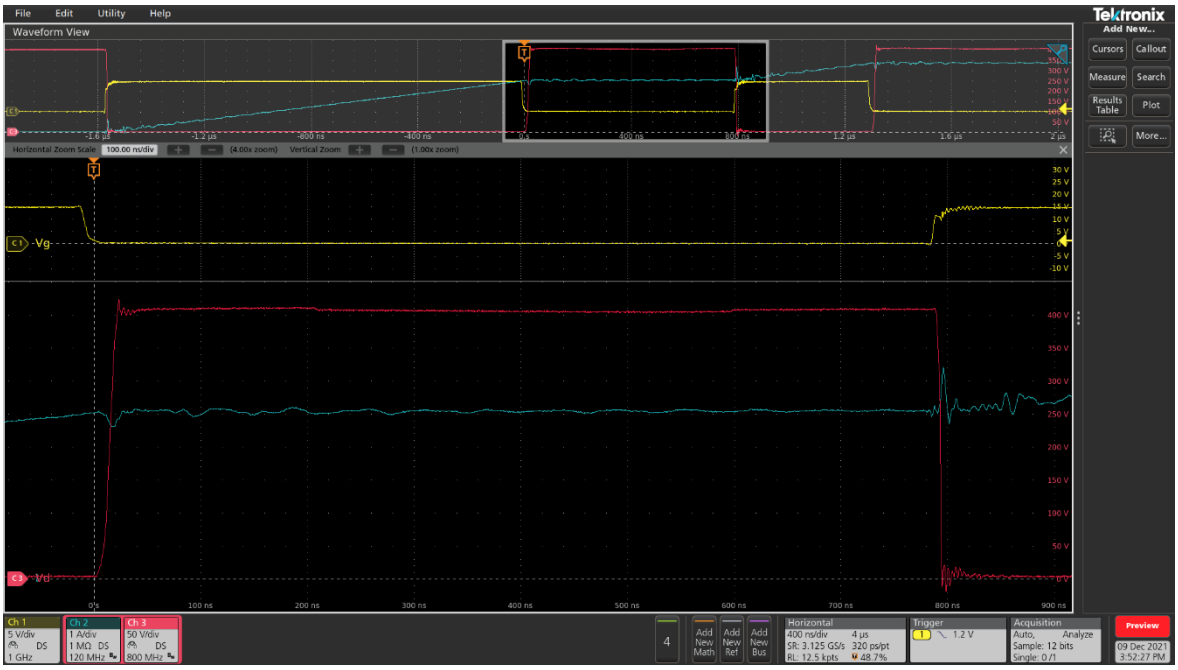

Figure 8 - Capture of 400 V, 5 A Double Pulse Test, Zoomed Switching Transition. (120 ns/div)

Red – V_{mid} 60 V/div, Yellow – Low Side Gate 5 V/div, Blue – Inductor Current 1 A/div

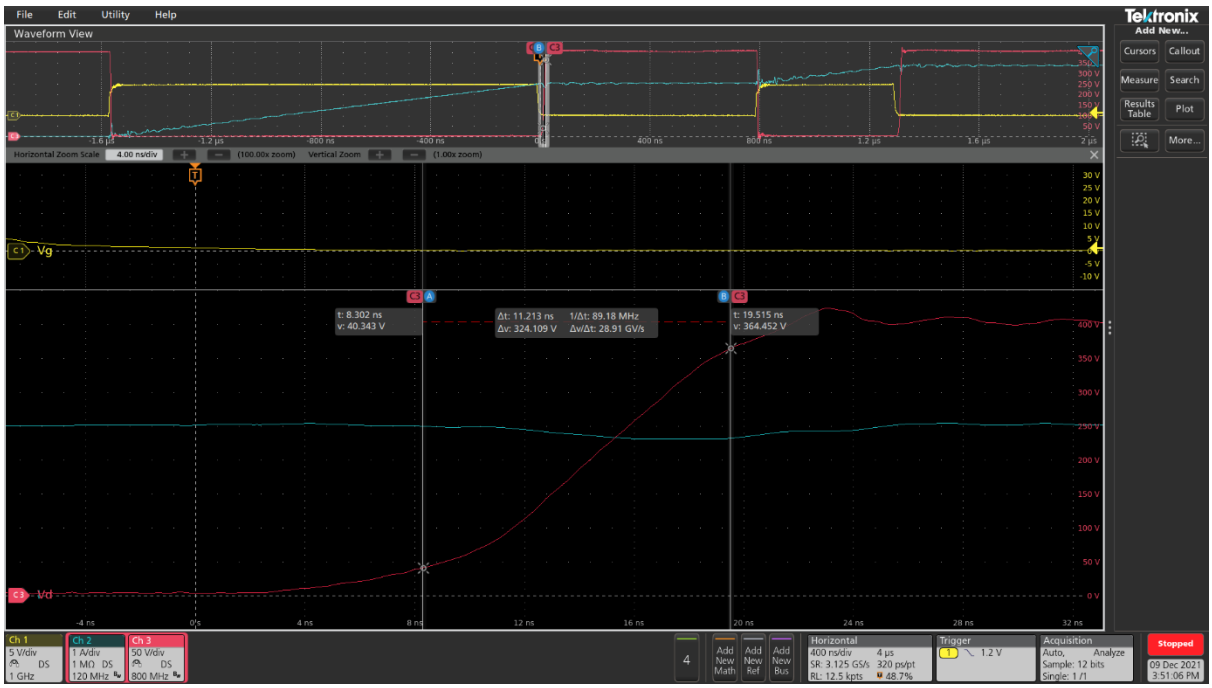

Figure 9 - Zoomed Rising Edge of V_{mid} in 400 V, 5 A Double Pulse Test

Red – V_{mid} 60 V/div, Yellow – Low Side Gate 5 V/div, Blue – Inductor Current 1 A/div

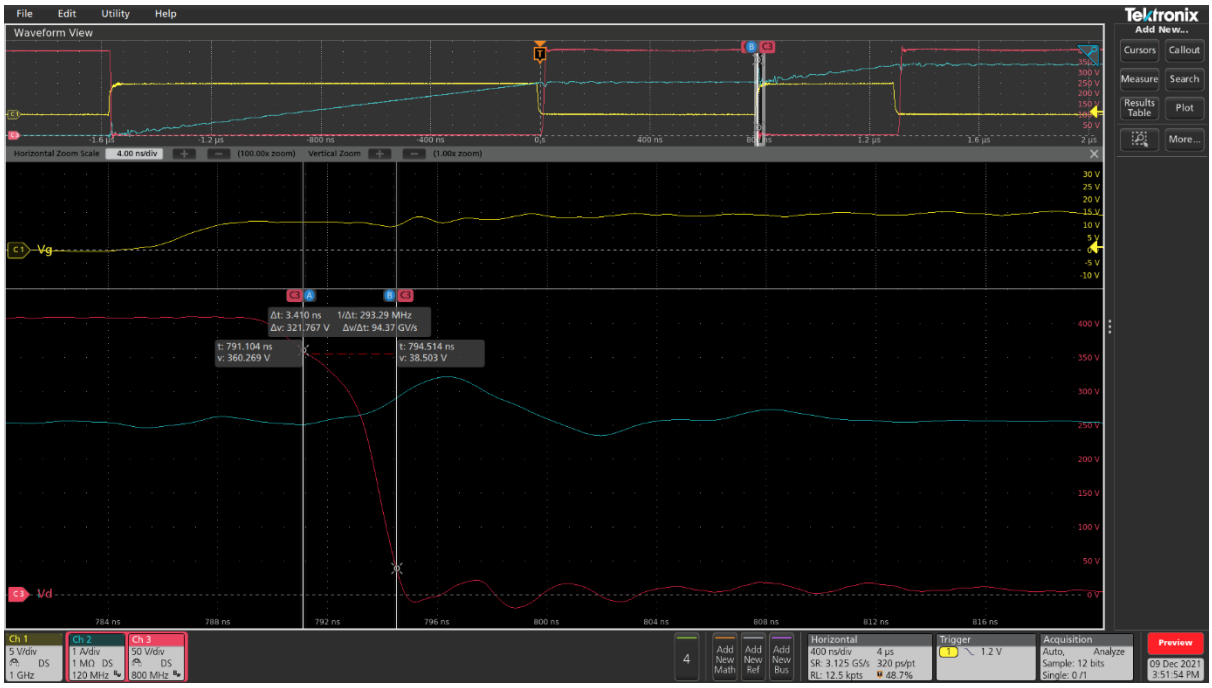

Figure 10 - Zoomed Falling Edge of Vmid in 400 V, 5 A Double Pulse Test

Red – V_{mid} 60 V/div, Yellow – Low Side Gate 5 V/div, Blue – Inductor Current 1 A/div

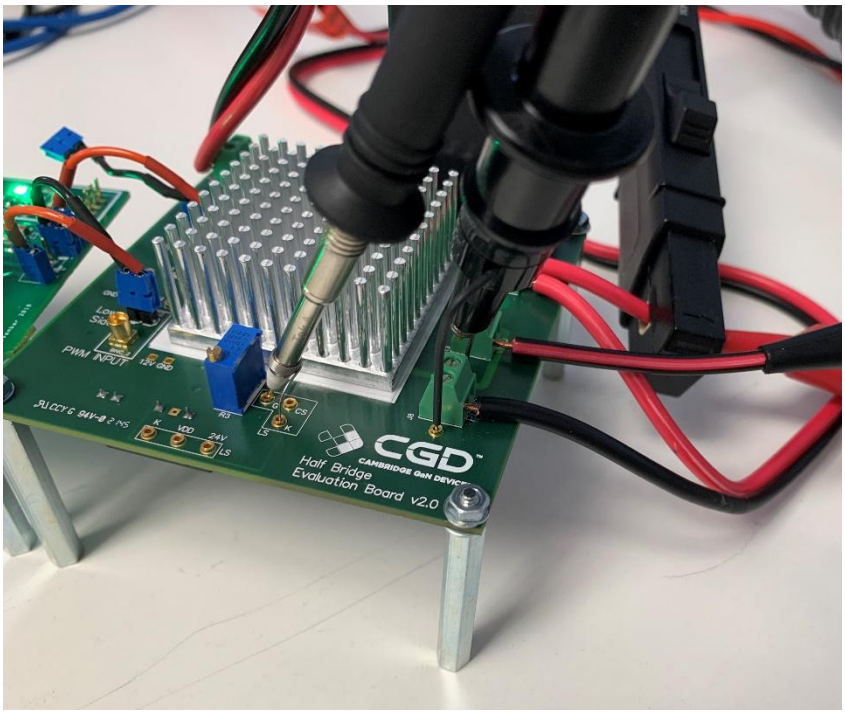

Figure 11 - Photograph of Probe Locations from Double Pulse Test for CGD-ASYEVB00801-01

5 Recommendations for Testing

- Low frequency oscillation or other noise may be seen using an oscilloscope to monitor the current sense signal. A common-mode choke may reduce the effect - e.g. wrap the oscilloscope probe cable around a closed EI core.

6 Schematics and Layout

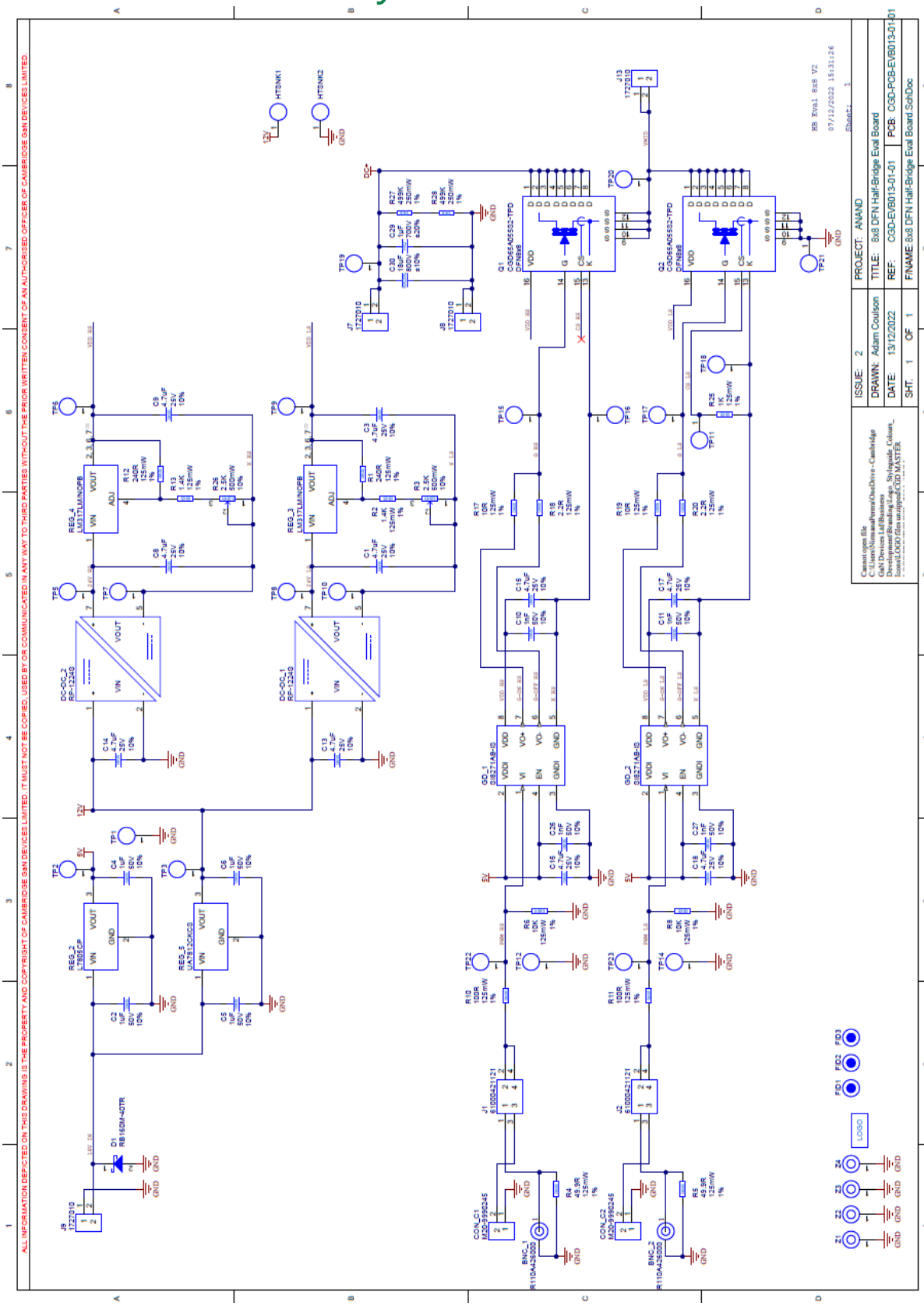

Figure 12 - CGD Half Bridge Evaluation Board Schematics DFN 8x8

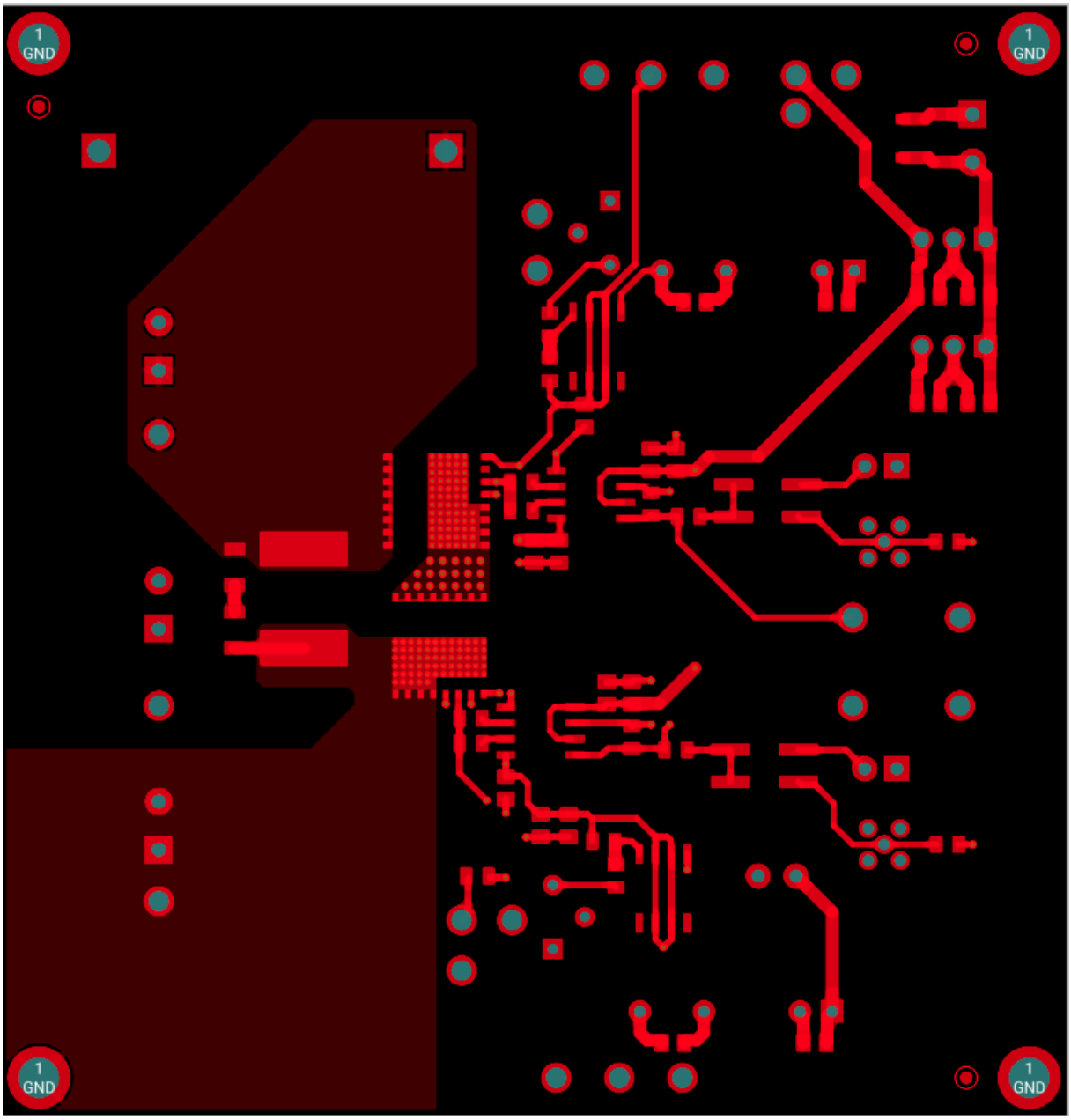

Figure 13 - CGD Half Bridge Evaluation Board Top Layer DFN 8x8

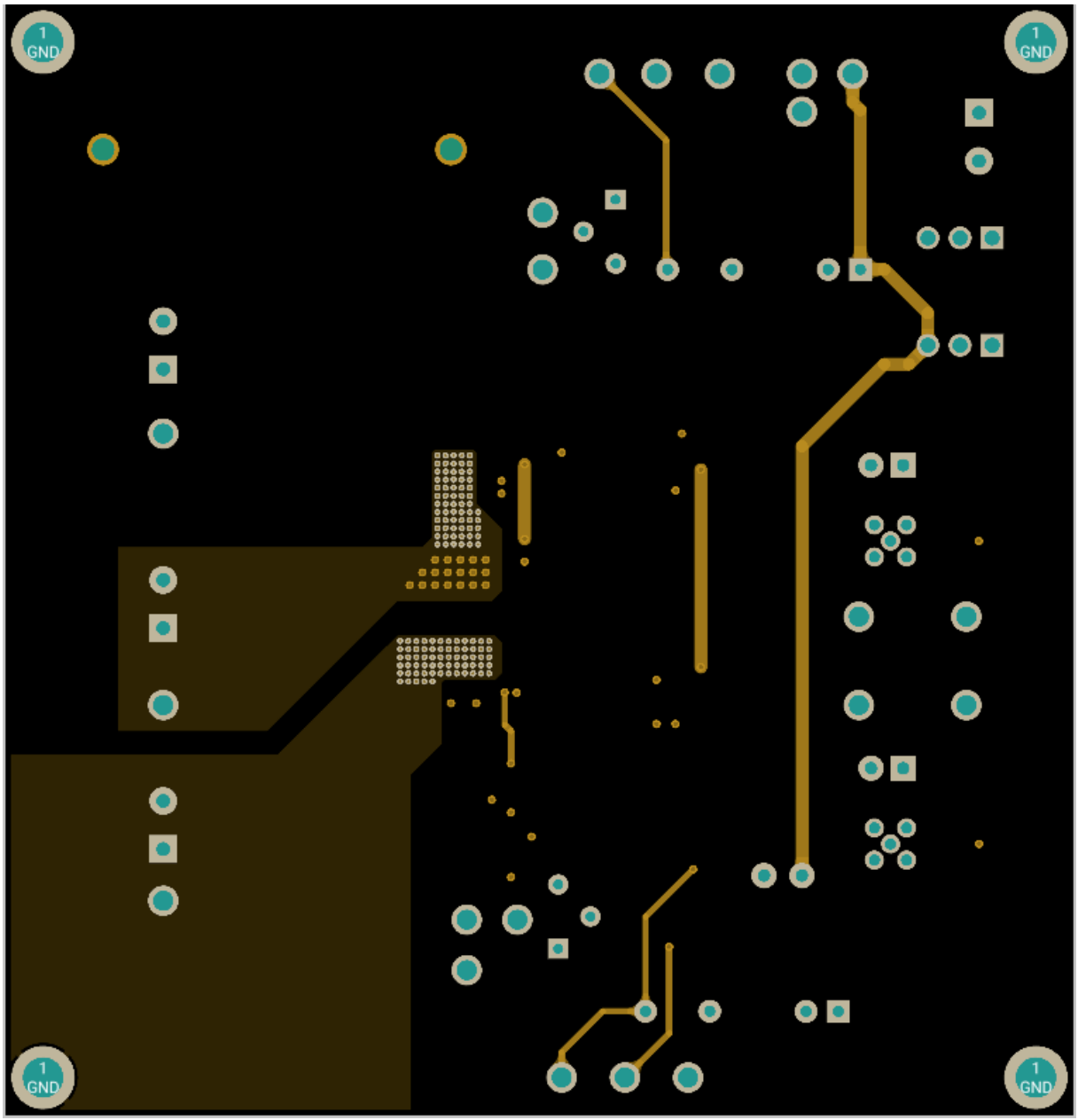

Figure 14 - CGD Half Bridge Evaluation Board Inner Layer 1 DFN 8x8

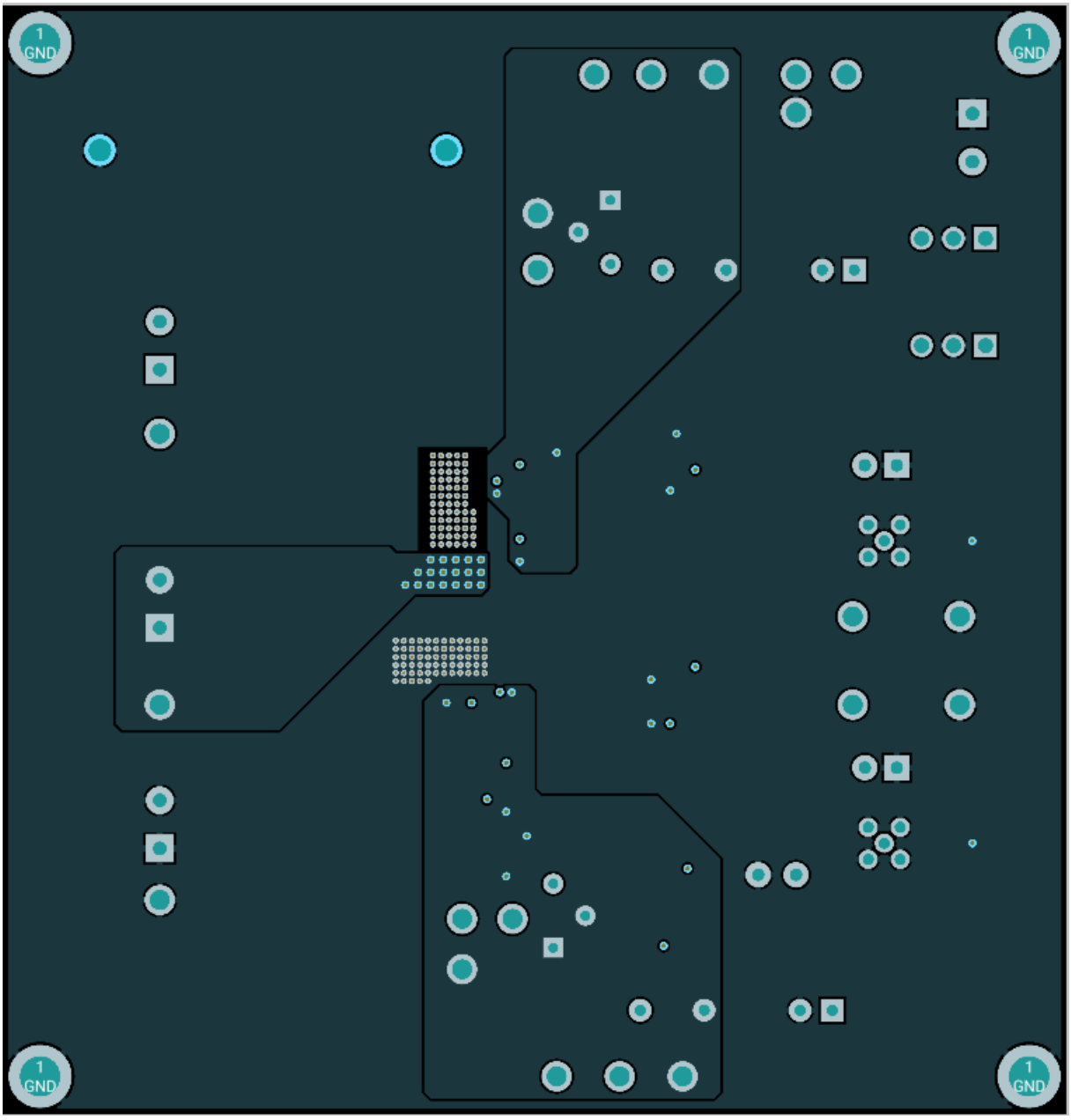

Figure 15 - CGD Half Bridge Evaluation Board Inner Layer 2 DFN 8x8

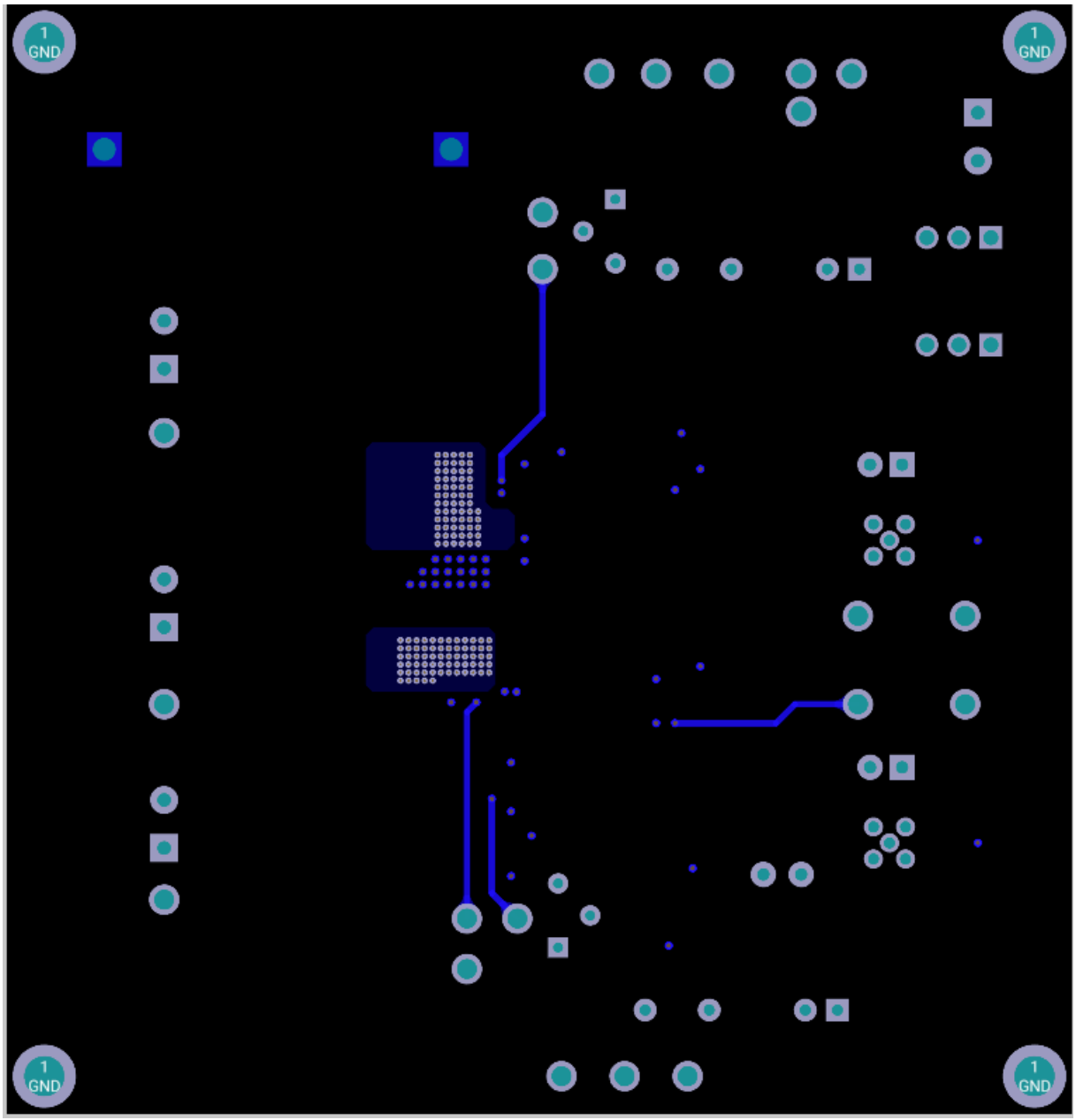

Figure 16 - CGD Half Bridge Evaluation Board Bottom Layer DFN 8x8

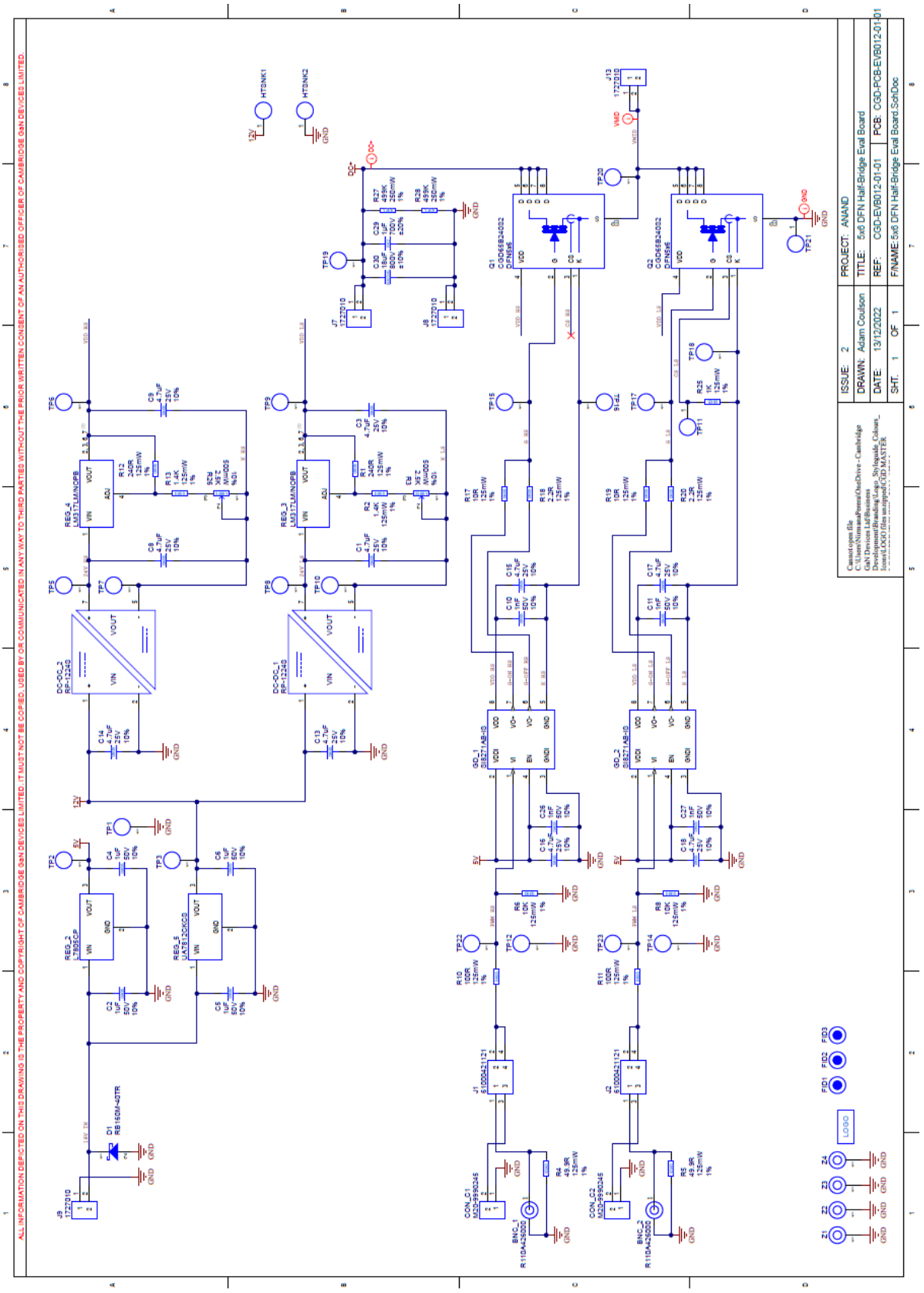

Figure 17 - CGD Half Bridge Evaluation Board Schematics DFN 5x6

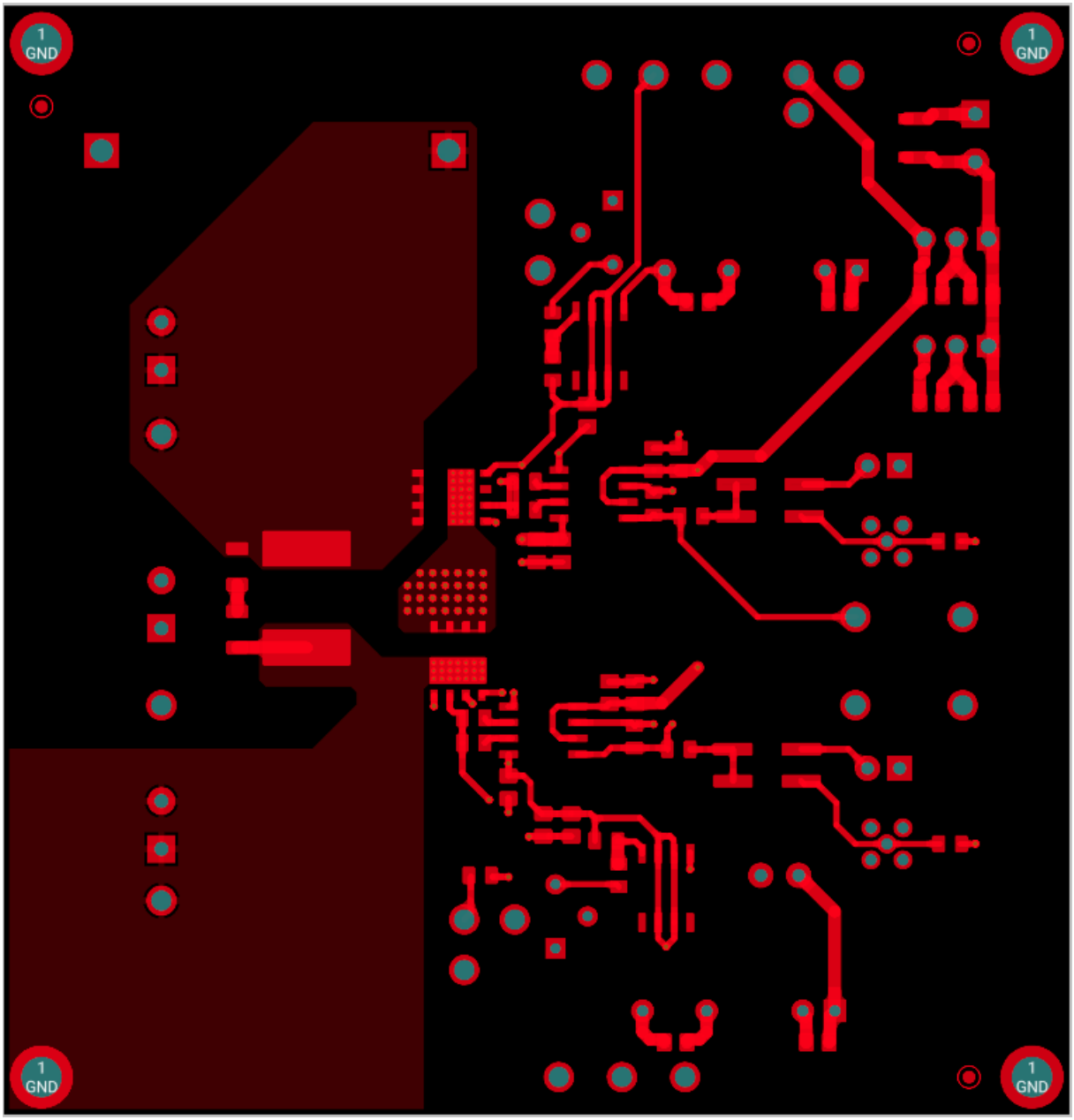

Figure 18 - CGD Half Bridge Evaluation Board Top Layer DFN 5x6

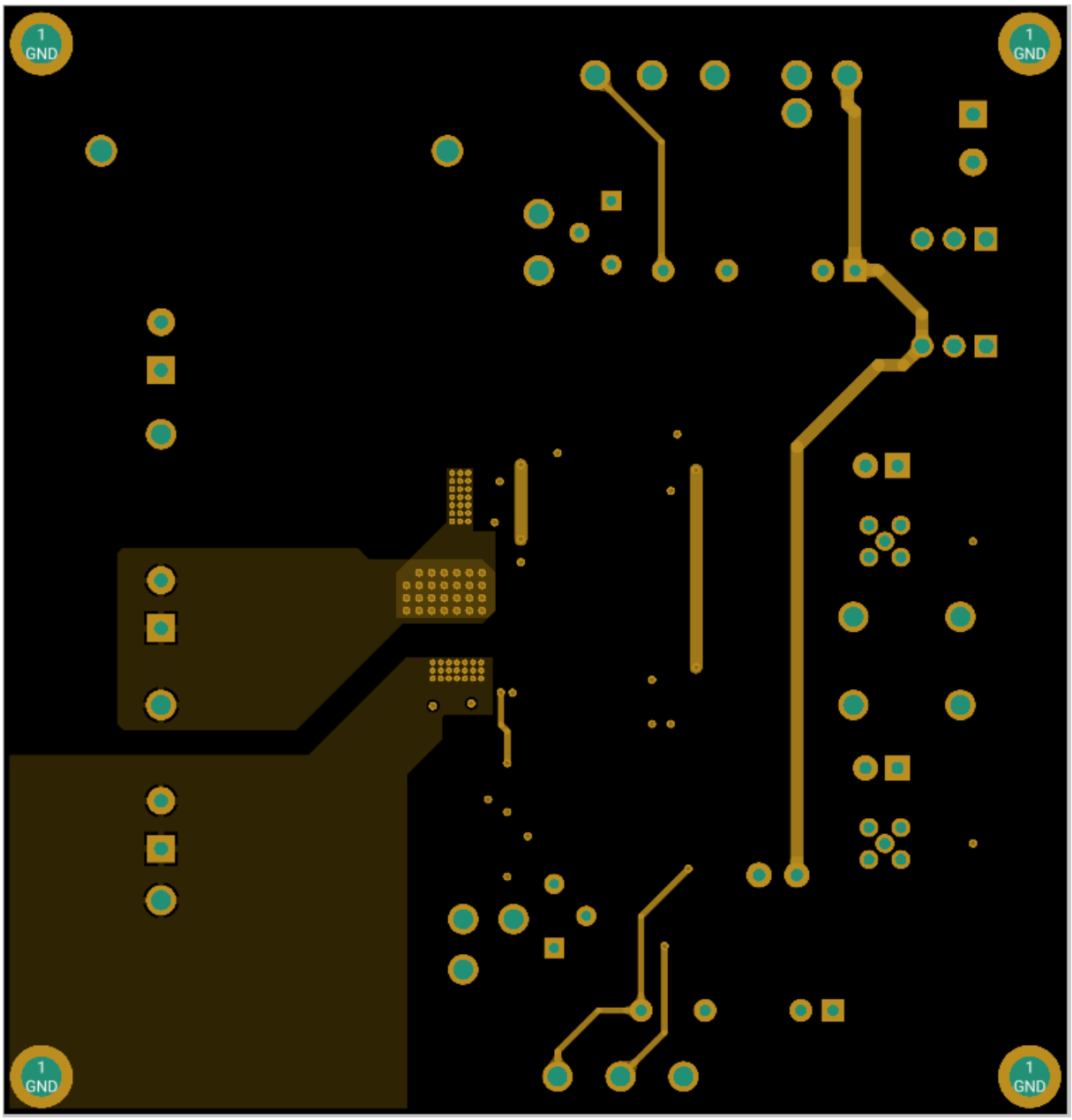

Figure 19 - CGD Half Bridge Evaluation Board Inner Layer 1 DFN 5x6

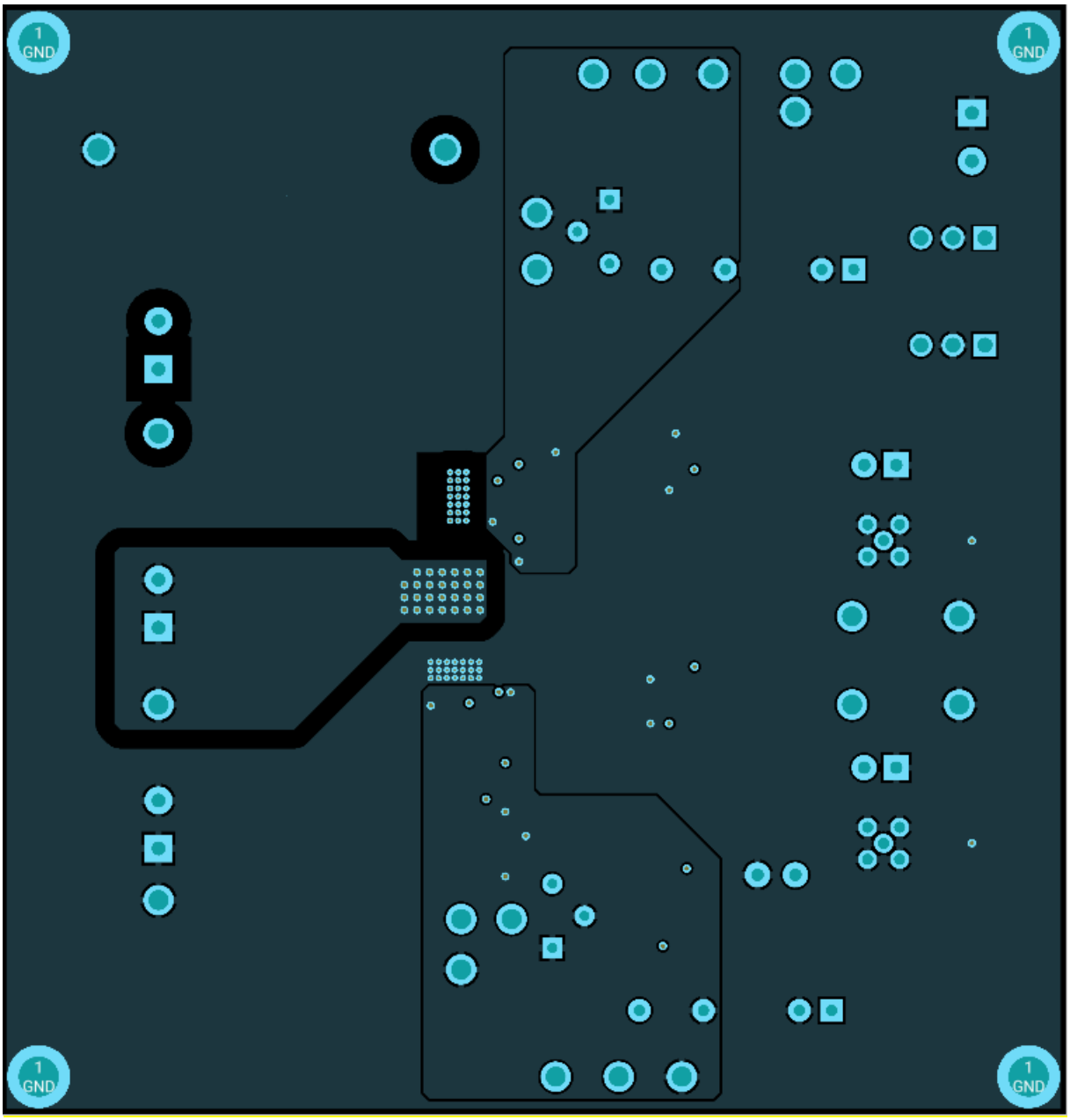

Figure 20 - CGD Half Bridge Evaluation Board Inner Layer 2 DFN 5x6

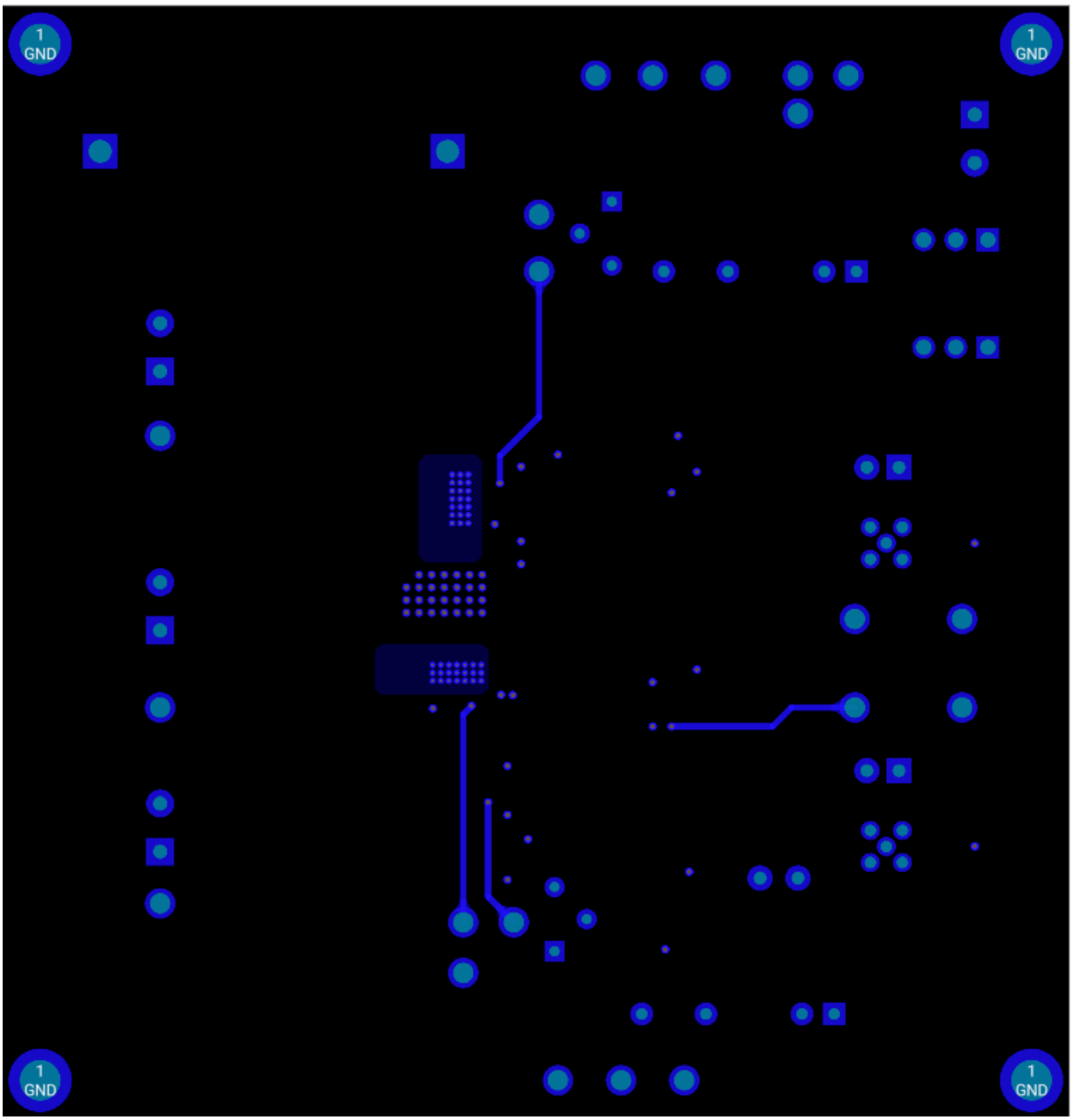

Figure 21 - CGD Half Bridge Evaluation Board Bottom Layer DFN 5x6

7 BOM

Part	Value	Package	Manufacturer	MPN
BNC_1	MMCX-Receptacle	MMCX-TH-5P	Radiall	R110A426000
BNC_2	MMCX-Receptacle	MMCX-TH-5P	Radiall	R110A426000
C1	4.7u	C0805	Kemet	C0805C475K3PACTU
C2	1u	C0805	Kemet	C0805C225M3RACTU
C3	4.7u	C0805	Kemet	C0805C475K3PACTU
C4	1u	C0805	Kemet	C0805C225M3RACTU
C5	1u	C0805	Kemet	C0805C225M3RACTU
C6	1u	C0805	Kemet	C0805C225M3RACTU
C8	4.7u	C0805	Kemet	C0805C475K3PACTU
C9	4.7u	C0805	Kemet	C0805C475K3PACTU
C10	1nF	C0805	KEMET	C0805C102K5RACTU
C11	1nF	C0805	KEMET	C0805C102K5RACTU
C13	4.7u	C0805	Kemet	C0805C475K3PACTU
C14	4.7u	C0805	Kemet	C0805C475K3PACTU
C15	4.7u	C0805	Kemet	C0805C475K3PACTU
C16	4.7u	C0805	Kemet	C0805C475K3PACTU
C17	4.7u	C0805	Kemet	C0805C475K3PACTU
C18	4.7u	C0805	Kemet	C0805C475K3PACTU
C26	1nF	C0805	KEMET	C0805C102K5RACTU
C27	1nF	C0805	KEMET	C0805C102K5RACTU
C29	1U	FA2	TDK	B58035U7105M062
C30	18u	EZPV_800V_18U	Panasonic	EZPV80186LTU
CON_C1	Header-2.54mm	2P-2.54MM-1ROW-VERT	Harwin	M20-9990245
CON_C2	Header-2.54mm	2P-2.54MM-1ROW-VERT	Harwin	M20-9990245
D1	40V	SOD123	ROHM	RB160M-40TR
DC-DC_1	12V	RECOM-DC/DC	RECOM	RP-1224S
DC-DC_2	12V	RECOM-DC/DC	RECOM	RP-1224S
Q1	CGD 650V GaN HEMT	DFN8X8/DFN5x6	CGD	-
Q2	CGD 650V GaN HEMT	DFN8X8/DFN5x6	CGD	-
GD_1	SI8271AB	SOIC08	Silicon Labs	SI8271AB-IS
GD_2	SI8271AB	SOIC08	Silicon Labs	SI8271AB-IS
J1	2X2_HEADER	2X2_2.54mm_SMD	Wurth	61000421121
J2	2X2_HEADER	2X2_2.54mm_SMD	Wurth	61000421121
J7	Screw-Terminal-3.81mm	2P-3.81MM	Phoenix Contact	1727010
J8	Screw-Terminal-3.81mm	2P-3.81MM	Phoenix Contact	1727010
J9	Screw-Terminal-3.81mm	2P-3.81MM	Phoenix Contact	1727010
J13	Screw-Terminal-3.81mm	2P-3.81MM	Phoenix Contact	1727010
R1	240R	R0805	Vishay	CRCW0805240RFKEA
R2	1.4k	R0805	Panasonic	ERJ6ENF1401V
R3	2.5K	3296Y	Bourns	3296Y-1-252LF
R4	49.9R	R0805	Vishay	CRCW080549R9FKEA
R5	49.9R	R0805	Vishay	CRCW080549R9FKEA
R6	10k	R0805	Panasonic	ERA6ARB103V
R8	10k	R0805	Panasonic	ERA6ARB103V
R10	100R	R0805	Panasonic	ERJ6ENF1000V
R11	100R	R0805	Panasonic	ERJ6ENF1000V
R12	240R	R0805	Vishay	CRCW0805240RFKEA

R13	1.4k	R0805	Panasonic	ERJ6ENF1401V
R17	10R	R0805	Panasonic	ERJ6ENF10R0V
R18	2.2R	R0805	Vishay	CRCW08052R20FKEA
R19	10R	R0805	Panasonic	ERJ6ENF10R0V
R20	2.2R	R0805	Vishay	CRCW08052R20FKEA
R25	1k	R0805	Multicomp Pro	MCWR08X1001FTL
R26	2.5K	3296Y	Bourns	3296Y-1-252LF
R27	499K	R1206	Bourns	CHV1206-FX-4993ELF
R28	499K	R1206	Bourns	CHV1206-FX-4993ELF
REG5	12V	TO220-3	TI	UA7812CKCS
REG_2	5V	TO-220FP-3	ST	L7805CP
REG_3	40V-1.2V	SOIC8	TI	LM317L-N
REG_4	40V-1.2V	SOIC8	TI	LM317L-N
TP2	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP3	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP5	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP6	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP7	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP8	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP9	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP10	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP11	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP12	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP14	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP15	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP16	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP17	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP18	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP19	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP20	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP21	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP22	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0
TP23	0.635..0.940mm	0305-2-15-15-47-27-10-0	Millmax	0305-2-15-15-47-27-10-0

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